

SGI DMediaPro™ DM2/DM3 Board
OpenML Media Library Owner's Guide

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Contents

List of Figures	ix
List of Tables	xi
About This Guide.xiii
Structure of This Guidexiv
Related Publicationsxiv
Product Support xv
Reader Comments xv
1. Features and Capabilities	1
DMediaPro Board Panel	2
Input/Output (I/O)	3
Supported Video Formats	3
Other Features	5
Theory of Operation	6
2. Installing the DMediaPro Board in a Silicon Graphics Octane2 Workstation	9
Checking Your Shipment	10
Checking Your Graphics Board	11
Upgrading the Operating System	12
Verifying the Operating System Installation	12
Installing the DMediaPro Software	12

Installing the DMediaPro Board 13
Preparing Your Workstation 13
Attaching the Wrist Strap. 15
Compression Connector Caution 16
Removing the XIO Tri-Module 17
Removing an XIO Option Board or Blank Panel 20
Attaching the DMediaPro Board to the Tri-Module 22
Reinstalling the XIO Tri-Module. 24
Powering On the Workstation 26
Verifying the Installation 27
3. Connecting the DMediaPro Board to VBOB 29
Getting Started 29
Connecting the DMediaPro Board to VBOB. 30
Setting Up VBOB for High Definition/Standard Definition I/O 31
Precautions on SGI Onyx/Origin Systems 32
4. Setting Up Audio Synchronization 33
Synchronizing Audio on an Octane2 Workstation 33
Synchronizing Audio on Onyx and Origin Systems 35
Setting Up the Audio Panel 37
Displaying AES Device Controls. 37
Setting the Default Input and Output to AES 37
Setting the Input and Output Signal Path 38
Setting the Output Sync Source 39
Other Configurations 44
5. Programming the DMediaPro Board 45
Programming Basics for the DMediaPro Board. 46

DMediaPro Controls	46
Path Controls and Jack Controls	47
Path Controls	47
Jack Controls	48
DMediaPro Control Summary	50
DMediaPro Default Path Controls	65
HD Default Input Path Controls	65
SD Default Input Path Controls	65
HD Default Output Path Controls	66
SD Default Output Path Controls	67
ML_TIMING	68
Input Timing Auto Detect	69
Genlock	69
Genlock Auto Detect.	72
ML_IMAGE_PACKING	72
ML_COLORSPACE	74
Color Spaces and Color Models	74
ML_COLORSPACE Control of Blanking	76
ML_COLORSPACE and Lookup Tables	76
ML_COLORSPACE Example	77
Field Dominance	78
EE Mode	79
Automatically Correcting for Output Underflow	80
Capturing Graphics to Video	80
DMediaPro Events.	81
Examples	84
Capturing 487 Line 525	84
Playback from Memory to Video	85
Re-sizing Field Height	86
Programmable Lookup Tables (LUTs)	88
FF Mode	89
Setting Controls on a Jack	90
Synchronizing Data Streams and Signals	92

Restrictions and Important Notes92
Index.95

List of Figures

Figure 1-1	DMediaPro Board Panel	2
Figure 1-2	DMediaPro Board Top-level Diagram	7
Figure 2-1	DMediaPro Board Shipment Components	10
Figure 2-2	Hardware Inventory List	11
Figure 2-3	Powering Off the Workstation	13
Figure 2-4	Removing the Monitor Cable	14
Figure 2-5	Attaching the Wrist Strap	15
Figure 2-6	Identifying the Compression Connector	16
Figure 2-7	Loosening the XIO Tri-Module Screws	17
Figure 2-8	Releasing the XIO Tri-Module	18
Figure 2-9	Removing the XIO Tri-Module	18
Figure 2-10	XIO Tri-Module.	19
Figure 2-11	Removing the Screws from the Blank Panel.	20
Figure 2-12	Removing the Blank Panel	21
Figure 2-13	Positioning the Board	22
Figure 2-14	Installing the Screws	23
Figure 2-15	Removing the Cap from a Compression Connector	23
Figure 2-16	Inserting the XIO Tri-Module.	25
Figure 2-17	Tightening the XIO Tri-Module Captive Screws	25
Figure 2-18	Reconnecting the Monitor Cable	26
Figure 2-19	Powering On the Workstation	26
Figure 2-20	Hardware Inventory List	27
Figure 3-1	Connecting the DMediaPro Board to VBOB.	30
Figure 3-2	Connecting the I/O Cables to VBOB.	31
Figure 4-1	Synchronizing Audio on an Octane2 Workstation	34
Figure 4-2	Synchronizing Audio on Onyx and Origin Systems	36
Figure 4-3	Selecting Preferences for the Output Device	39

Figure 4-4	Synchronizing the Octane2 Internal Audio40
Figure 4-5	Synchronizing a Single PCI Digital Audio Board on an Onyx or Origin System41
Figure 4-6	Synchronizing Two PCI Digital Audio Boards on an Onyx/Origin System (RAD 1.AES Out Preferences)42
Figure 4-7	Synchronizing Two PCI Digital Audio Boards on an Onyx/Origin System (RAD 2.AES Out Preferences)43
Figure 5-1	Setting Up Paths.47
Figure 5-2	Using a Jack Control to Change the EE Mode During a Transfer48
Figure 5-3	Color Space Conversion Example77
Figure 5-4	Fields and Frames for SMPTE 274M78

List of Tables

Table 1-1	Supported Video Timings	4
Table 1-2	Supported Packing Modes	5
Table 5-1	HD/SD Input and Output Paths	50
Table 5-2	DMediaPro Board Control Parameters/Value(s) and Use.	53
Table 5-3	Supported HD Input/Output Timings	70
Table 5-4	VL/ML Packing Conversions.	72
Table 5-5	DMediaPro Events	81
Table 5-6	Error Status Values for ML_EVENT_VIDEO_SYNC_LOST (output path)	83

About This Guide

Welcome to DMediaPro Video, an SGI technology!

The DMediaPro DM2 and DM3 Boards (for Silicon Graphics Octane2 V10 and V12 workstations, SGI Onyx 2/Origin 2000 systems, and SGI Onyx 3000/Origin 3000 systems respectively), transmit and receive uncompressed High Definition video and Standard Definition video in real-time. In the future, the DMediaPro DM2 and DM3 boards (referred to as DMediaPro Board throughout this guide) will also be compatible with other SGI systems.

For Onyx 2/Origin 2000 and Onyx 3000/Origin 3000 systems (and future Onyx/Origin compatible products), the DMediaPro Board must be installed by an SGI field installer. To install the board in an Octane2 workstation, follow the installation instructions in Chapter 2 of this guide.

Note: This option board requires IRIX 6.5.11 (with any required patches) or later.

You control board features using the *OpenML Media Library Software Development Kit (ML)*. For a description of ML device-independent calls and controls, see the *OpenML Media Library Software Development Kit Programmer's Guide* (007-4504-00x).

This guide is provided for the sophisticated video user in a professional or research environment. You should be familiar with video standards, the operation of the applicable SGI system or workstation, and the ML-related information in the *OpenML Media Library Software Development Kit Programmer's Guide*.

Structure of This Guide

This guide includes the following chapters and appendices:

- Chapter 1, “Features and Capabilities,” describes the main components of the DMediaPro Board, and includes a general overview of product features.
- Chapter 2, “Installing the DMediaPro Board in a Silicon Graphics Octane2 Workstation,” shows you how to install the board in an Octane2 Tri-Module.
- Chapter 3, “Connecting the DMediaPro Board to VBOB,” shows you how to set up High Definition and Standard Definition Input/Output (I/O) using the SGI Video Breakout Box (VBOB).
- Chapter 4, “Setting Up Audio Synchronization,” shows you how to synchronize audio with video when using the DMediaPro Board in a typical studio configuration with a tape deck.
- Chapter 5, “Programming the DMediaPro Board,” shows you how to use ML and device-specific controls to program the board.

Related Publications

In addition to this guide, the *OpenML Media Library Software Development Kit Programmer’s Guide* (007-4504-00x) and the *SGI Video Breakout Box Owner’s Guide* (007-4243-00x), are shipped with the DMediaPro Board. If you are using an SGI PCI Digital Audio Board, see the *SGI PCI Digital Audio Board Installation Guide* (007-3502-00x).

It is also a good idea to have your system owner’s guide available. If you do not have these guides handy, you can access online documentation as follows:

- In the IRIS InSight Library, select Toolchest > Help > Online Books > SGI EndUser or SGI Admin, and select the applicable guide.
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Features and Capabilities

This chapter describes the features and capabilities of the DMediaPro Board. The following topics are covered:

- “DMediaPro Board Panel” on page 2
- “Input/Output (I/O)” on page 3
- “Supported Video Formats” on page 3
- “Other Features” on page 5
- “Theory of Operation” on page 6

DMediaPro Board Panel

Figure 1-1 shows the DMediaPro Board with its connectors and LEDs. The board ships with two Low Voltage Differential Signaling (LVDS) cables that interface with the SGI Video Breakout Box (VBOB).

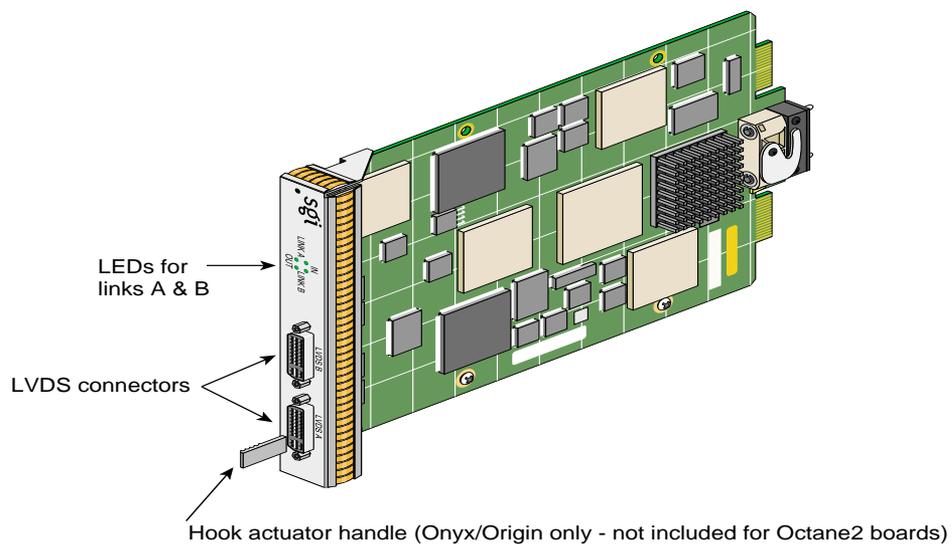


Figure 1-1 DMediaPro Board Panel

Input/Output (I/O)

The DMediaPro system uses the VBOB for analog genlock connections and Serial Digital Interface (SDI) High Definition (HD) and Standard Definition (SD) video I/O.

Note: For information on I/O and genlock timing features, see Chapters 3 and 5 in this guide. For a complete description of the VBOB, including all the I/O connectors, see the *SGI Video Breakout Box Owner's Guide*.

Supported Video Formats

The DMediaPro Board supports video formats defined by the Advanced Television Standards Committee (ATSC), as well as several formats defined for High Definition digital motion pictures and post production. In addition, the board supports several Standard Definition formats. These formats can have pixel clocks of up to 74.25 MHz. These formats include support for:

- 1080p, 1080i, 720p, 576i, and 480i video formats
- 23.98, 24, 25, 29.97, 30, 59.94, and 60 Hz vertical rates
- 16 x 9 and 4 x 3 aspect ratios

Examples of supported formats are SMPTE 274M (interlaced and progressive), SMPTE 296 (progressive), ITU-R BT.601-5 (interlaced), SMPTE 260M, and SMPTE 240M.

Note: ITU-R BT.601-5 is also known as Rec. 601 and CCIR 601.

Table 1-1 lists the DMediaPro Board video timings that are supported for the first release of the board.

Note: In the third column of the table, the prefix, ML_TIMING_ should appear before each timing, but was omitted to avoid redundancy.

Table 1-1 Supported Video Timings

Description	Frame Rate	Timing
1920x1080 interlaced	30/1.001 Hz	1125_1920x1080_5994i
1280x720 progressive	60/1.001 Hz	750_1280x720_5994p
1280x720 progressive	60 Hz	750_1280x720_60p
1920x1080 interlaced	25 Hz	1125_1920x1080_50i
1920x1080 interlaced	30 Hz	1125_1920x1080_60i
1920x1080 progressive	24 Hz	1125_1920x1080_24p
1920x1080 progressive	24/1.001 Hz	1125_1920x1080_2398p
1920x1080 progressive	25 Hz	1125_1920x1080_25p
1920x1080 progressive segmented frame	25 Hz	1125_1920x1080_25PsF
1920x1080 progressive segmented frame	24 Hz	1125_1920x1080_24PsF
1920x1080 progressive segmented frame	24/1.001 Hz	1125_1920x1080_2398PsF
1920x1035 interlaced	30/1.001 Hz	1125_1920x1035_5994i
720 x 487 (NTSC)	30/1.001 Hz	525
720 x 576 (PAL)	25 Hz	625

In Progressive segmented Frame (PsF) formats, the progressive frame is transmitted as two fields that are from the same progressive scan, while in interlaced formats the two fields are temporally displaced.

All formats are 8-bit or 10-bit. These formats are used for content creation and telecine output, and support serial-parallel conversion.

Other Features

The DMediaPro Board includes the following features:

- Programmable field size (see “Re-sizing Field Height” on page 86).
- YCrCb with 8- or 10-bits per component (4:2:2 or 4:4:4 sampling rates).
- Alpha channel support.
- Video interface support for RGB 8- or 10- bits.
- Support for up to 64 bits/pixel RGB in memory.
- Real-time “transparent” color space conversion in ITU-R Rec. 601, ITU-R Rec. 709, SMPTE 240M, and key scaling.
- User-programmable horizontal and vertical phase adjustment of the output video.
- Unadjusted System Time (UST) and Media Stream Count (MSC) support on input and output.
- Gamma correction support through user-downloadable 13-bit-wide lookup table.
- 3/2 pulldown mode on output.
- Full Frame mode supported at SD rates (270 MB/sec) for compressed image I/O (for HDcam, DVcam, and other compressed HD formats).
- Packing modes (see Table 1-2). For VL/ML packing conversions, see “ML_IMAGE_PACKING” on page 72.

Table 1-2 Supported Packing Modes

ML_IMAGE_PACKING	ML_IMAGE_SAMPLING
ML_PACKING_8	ML_SAMPLING_422
ML_PACKING_8_3214	ML_SAMPLING_422
ML_PACKING_10	ML_SAMPLING_422
ML_PACKING_10_3214	ML_SAMPLING_422
ML_PACKING_10in16L	ML_SAMPLING_422
ML_PACKING_10in16L_3214	ML_SAMPLING_422
ML_PACKING_10in16R	ML_SAMPLING_422

Table 1-2 (continued) Supported Packing Modes

ML_IMAGE_PACKING	ML_IMAGE_SAMPLING
ML_PACKING_10in16R_3214	ML_SAMPLING_422
ML_PACKING_10_10_10_2	ML_SAMPLING_4224
ML_PACKING_10_10_10_2_3214	ML_SAMPLING_4224
ML_PACKING_8	ML_SAMPLING_444
ML_PACKING_8_R	ML_SAMPLING_444
ML_PACKING_S12in16L	ML_SAMPLING_444
ML_PACKING_S12in16R	ML_SAMPLING_444
ML_PACKING_8	ML_SAMPLING_4444
ML_PACKING_8_R	ML_SAMPLING_4444
ML_PACKING_10_10_10_2	ML_SAMPLING_4444
ML_PACKING_10_10_10_2_R	ML_SAMPLING_4444

Theory of Operation

The DMediaPro Board (DM2 and DM3) interfaces High Definition (HD), Standard Definition (SD), and Serial Digital Transport Interface (SDTI) video formats to the SGI XIO bus. The board is the second generation of the HD I/O architecture.

The DMediaPro Board provides a full-duplex, dual-link, High Definition (HD) and Standard Definition (SD) video interface between the SGI 400 MHz Crosstalk XIO bus and the DMediaPro LVDS links. The LVDS links run at seven times the programmed video rates, from 189 MHz to 519.75 MHz, corresponding to seven times the 27 MHz to 74.25 MHz video link rates. The board uses an internal 100 MHz bus architecture, which is common to both the SGI HD I/O Board and the SGI Infinite Reality graphics systems. This architecture is based on the SGI "XG" ASIC. The board's video input and output pipes interface to this internal bus through DMA engines contained in the SGI "GIF" FPGA. GIF also controls all other FPGAs through the local bus controller and the PIO unit. The various packings and color spaces are supported by the packers, unpackers, and the input and output color space converter FPGAs.

The board also supports Downloadable Lookup Tables (LUTs) for linear, log, and gamma correction. Video input and output format and control are contained in the VIF and HDOC FPGAs, respectively. The CLINK FPGA contains the LVDS channel link control and the status logic.

Figure 1-2 is a simplified top-level diagram of the DMediaPro Board.

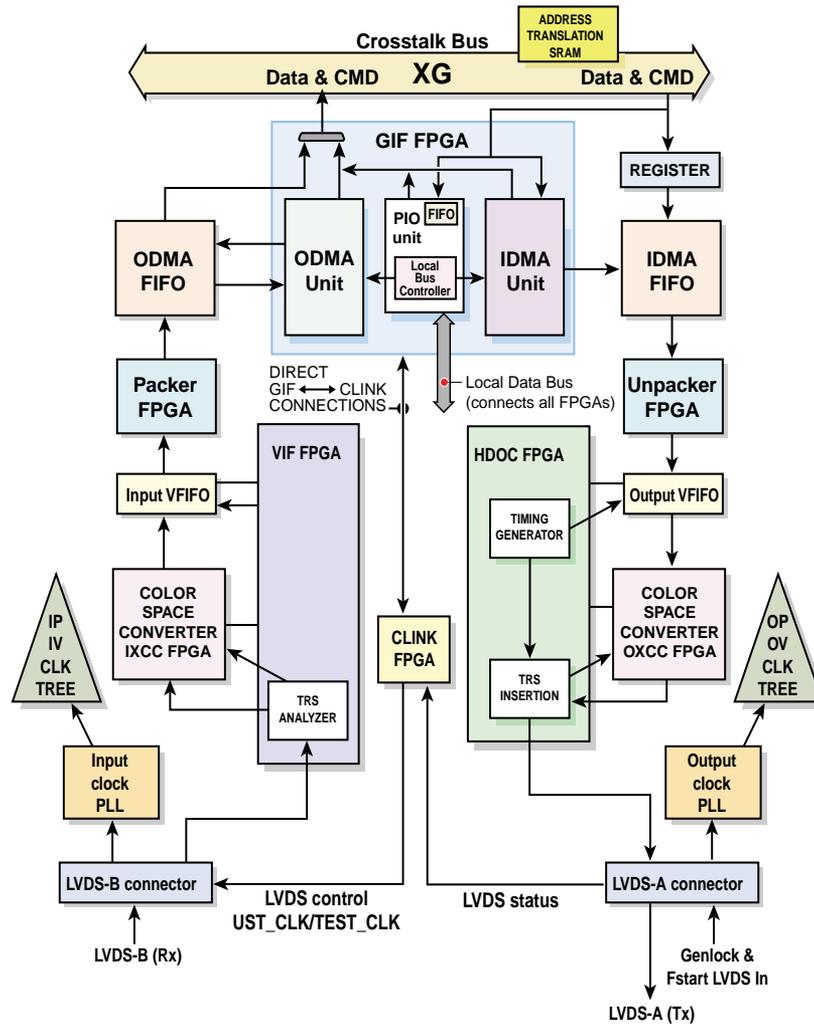


Figure 1-2 DMediaPro Board Top-level Diagram

Installing the DMediaPro Board in a Silicon Graphics Octane2 Workstation

This chapter shows you how to install the DMediaPro Board in an Octane2 VPro V10 or V12 workstation (or an upgraded Octane workstation). For this type of installation, your upgraded Octane or Octane2 must have a properly installed V10 or V12 Graphics Board (with frontplane Xbow 1.4 or higher). In addition, your workstation must have a 400 MHz processor, 256 MB of system memory, the appropriate number of fiber channel boards for your bandwidth requirements, and a PCI module. For fiber channel board requirements, contact your SGI sales representative.

Note: If you have a compatible SGI Onyx or SGI Origin system, skip this section. On these systems, the DMediaPro Board must be installed by an SGI field installer.

The following topics are covered:

- “Checking Your Shipment” on page 10
- “Checking Your Graphics Board” on page 11
- “Upgrading the Operating System” on page 12
- “Installing the DMediaPro Software” on page 12
- “Installing the DMediaPro Board” on page 13
- “Verifying the Installation” on page 27

Checking Your Shipment

Make sure your shipment includes the items shown in Figure 2-1.

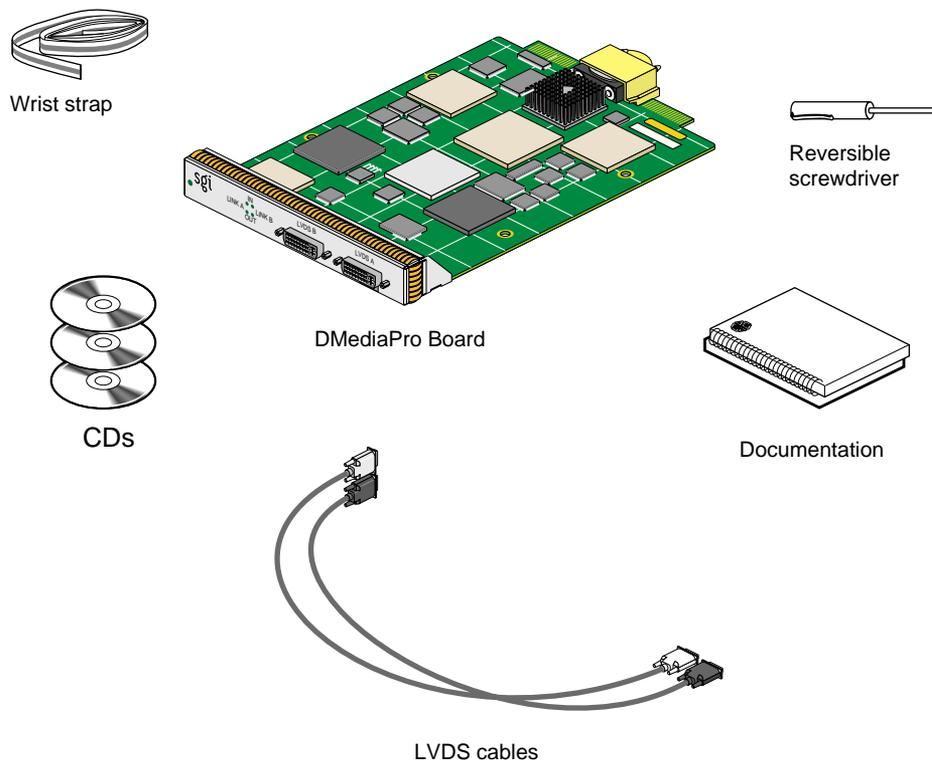


Figure 2-1 DMediaPro Board Shipment Components

Checking Your Graphics Board

To use the DMediaPro Board, your workstation must have a VPro V10 or V12 Graphics Board installed. To verify your graphics board (and all the other required hardware), follow these steps:

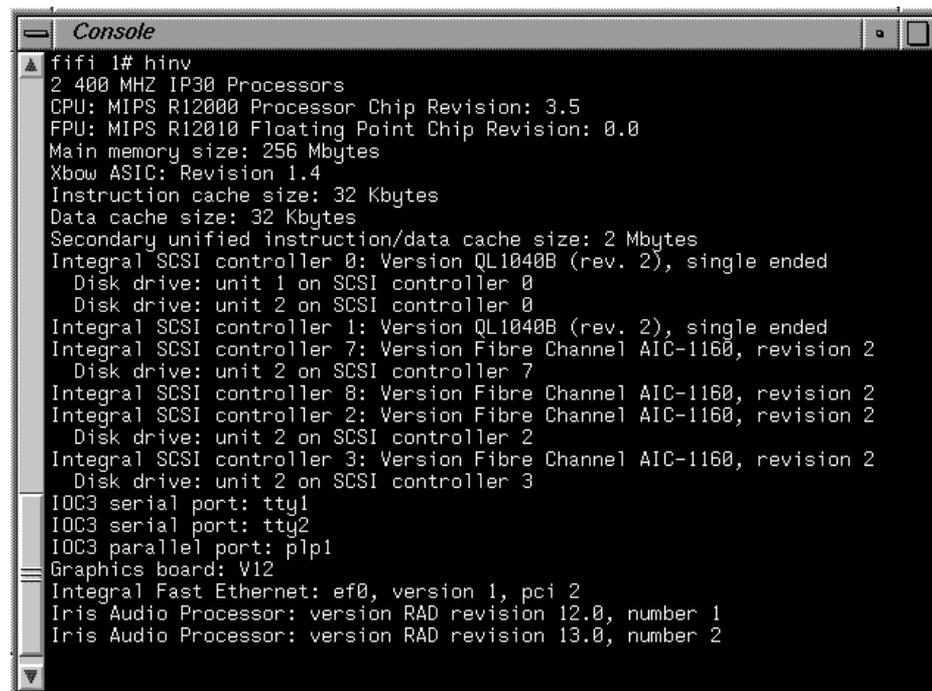
1. Open a UNIX shell.
2. At the prompt, enter `hinv`.

The hardware inventory list appears, as shown in the example in Figure 2-2.

3. Look for the following line describing your graphics board.

Graphics board: V10 or V12

If V10 or V12 does not appear for your graphics board, you cannot use the DMediaPro Board. For more information, contact your authorized SGI sales representative.



```
fifi 1# hinv
2 400 MHZ IP30 Processors
CPU: MIPS R12000 Processor Chip Revision: 3.5
FPU: MIPS R12010 Floating Point Chip Revision: 0.0
Main memory size: 256 Mbytes
Xbow ASIC: Revision 1.4
Instruction cache size: 32 Kbytes
Data cache size: 32 Kbytes
Secondary unified instruction/data cache size: 2 Mbytes
Integral SCSI controller 0: Version QL1040B (rev. 2), single ended
  Disk drive: unit 1 on SCSI controller 0
  Disk drive: unit 2 on SCSI controller 0
Integral SCSI controller 1: Version QL1040B (rev. 2), single ended
Integral SCSI controller 7: Version Fibre Channel AIC-1160, revision 2
  Disk drive: unit 2 on SCSI controller 7
Integral SCSI controller 8: Version Fibre Channel AIC-1160, revision 2
Integral SCSI controller 2: Version Fibre Channel AIC-1160, revision 2
  Disk drive: unit 2 on SCSI controller 2
Integral SCSI controller 3: Version Fibre Channel AIC-1160, revision 2
  Disk drive: unit 2 on SCSI controller 3
IOC3 serial port: tty1
IOC3 serial port: tty2
IOC3 parallel port: plp1
Graphics board: V12
Integral Fast Ethernet: ef0, version 1, pci 2
Iris Audio Processor: version RAD revision 12.0, number 1
Iris Audio Processor: version RAD revision 13.0, number 2
```

Figure 2-2 Hardware Inventory List

Upgrading the Operating System

To install the DMediaPro Board, your workstation must have IRIX 6.5.11 (and any required patches) or later installed. To install IRIX 6.5.11 or later, follow the software installation instructions included with the IRIX Upgrade CDs.

Verifying the Operating System Installation

To verify the installation of IRIX 6.5.11 or later, enter the following in a command line window: `uname -R`.

Installing the DMediaPro Software

To install the DMediaPro software, insert the DMediaPro CD in your CDROM drive, then open a UNIX shell and follow these steps:

1. Install the ML images as follows:
 - Enter `inst -A -f /CDROM/dist/ml`
The system performs a pre-installation check, verifies space requirements, installs the dmsdk images, and then verifies the installation.
2. Install the xtdigvid images as follows:
 - Enter `inst -A -f /CDROM/dist/ml_xtdigvid`
The system performs a pre-installation check, verifies space requirements, installs the xtdigvid images, and then verifies the installation.
3. Shutdown your workstation.

Note: The above procedure installs all the software that is required for both users and developers. If you want to develop applications that run under dmSDK, go to Chapter 5, "Programming the DMediaPro Board," for additional instructions and programming information.

Installing the DMediaPro Board

This section shows you how to install the DMediaPro Board in an Octane2 workstation with a VPro V10 or V12 Graphics Board (referred to as the VPro Graphics Board in the following instructions).

Preparing Your Workstation

To prepare your workstation, follow these steps:

1. Open the cover and press the power button (see A in Figure 2-3) to power off your workstation.
2. Unplug the power cable (B).
3. Press the monitor power switch (C) to power off your monitor.

Wait five minutes before removing the XIO Tri-Module.

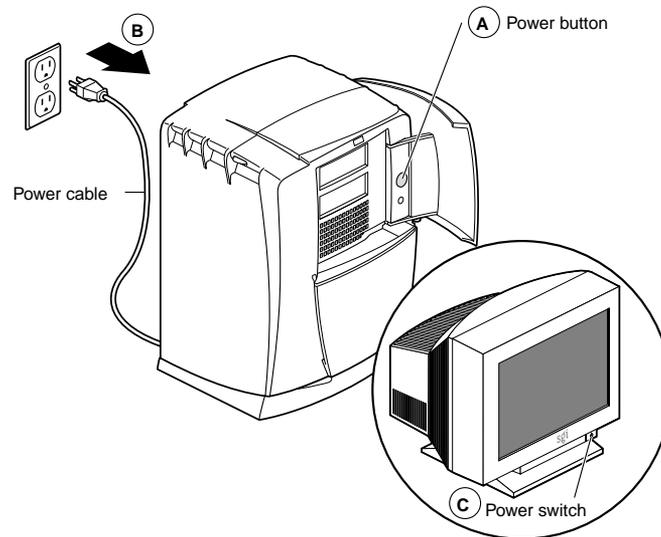


Figure 2-3 Powering Off the Workstation



Warning: The heat sinks on the XIO boards get very hot. Wait 5 minutes after powering off the workstation before you remove the XIO Tri-Module. Test before touching any of the XIO boards.

4. Remove all the cables from the XIO Tri-Module (only one is shown in Figure 2-4), then attach the wrist strap, as described in the next section.

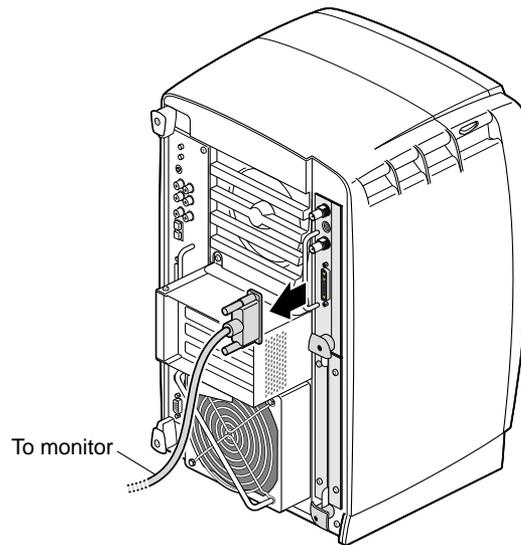


Figure 2-4 Removing the Monitor Cable

Attaching the Wrist Strap



Caution: The components inside the workstation are extremely sensitive to static electricity; you must wear the wrist strap while replacing parts inside the workstation.

To attach the wrist strap, follow these steps:

1. Unroll the first two folds of the band (see A in Figure 2-5).
2. Wrap the exposed adhesive side firmly around your wrist (B), unroll the rest of the band, and then peel the liner from the copper foil at the opposite end.
3. Attach the copper foil to any exposed electrical ground, such as a metal part of the workstation (C).

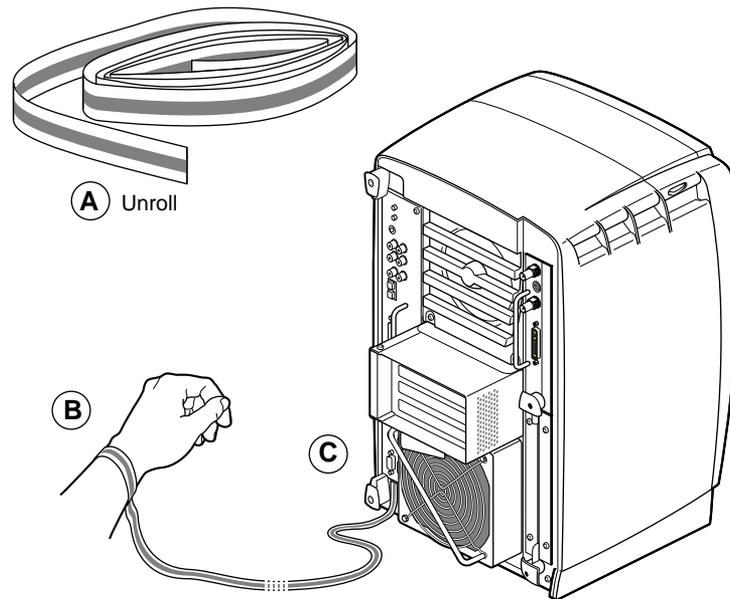


Figure 2-5 Attaching the Wrist Strap

Compression Connector Caution



Caution: The compression connectors on all XIO graphics boards and most option boards are very delicate and easily damaged. Do not touch or bump the gold bristled pad (see Figure 2-6). The connectors are on the side opposite the handles. Do not grab the back of the XIO module when you remove it, or the compression connectors may be damaged.

Always place caps on all compression connectors after removing XIO boards. Caps are included with your workstation. Remove all caps from the compression connectors before installing XIO boards in your workstation.

Before you remove the XIO Tri-Module, read “Care and Cleaning of the Compression Connector” in the appendix section of your *Octane or Octane2 Workstation Owner’s Guide*.

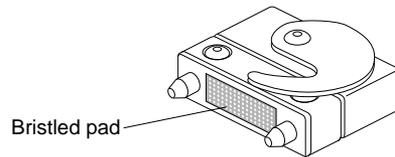


Figure 2-6 Identifying the Compression Connector

Removing the XIO Tri-Module

To remove the XIO Tri-Module, follow these steps:

1. Loosen the two captive screws in the XIO Tri-Module sliding handles with the supplied Phillips screwdriver, as shown in Figure 2-7, until the screws are disconnected from the chassis.



Warning: The heat sinks on the XIO boards get very hot. Wait 5 minutes after powering off your workstation before you remove the XIO Tri-Module. Test before touching any of the XIO boards.

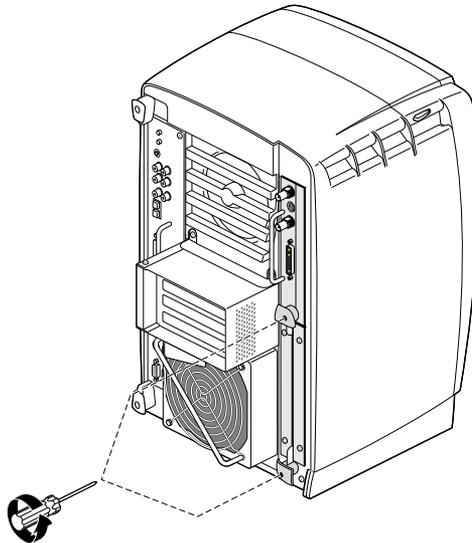


Figure 2-7 Loosening the XIO Tri-Module Screws

2. Grasp the handles and pull them until the XIO Tri-Module protrudes about an inch from the chassis, as shown in Figure 2-8.

The handles and XIO Tri-Module move out about one inch before the I/O panels move.

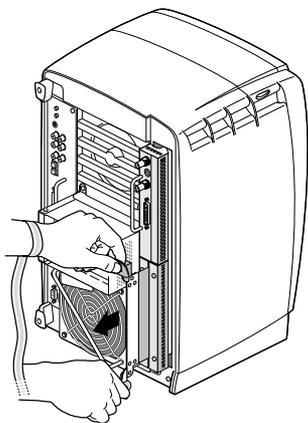


Figure 2-8 Releasing the XIO Tri-Module

3. Grasp the XIO Tri-Module by the immovable handle, and support the base of the module as you remove it from the chassis, as shown in Figure 2-9.

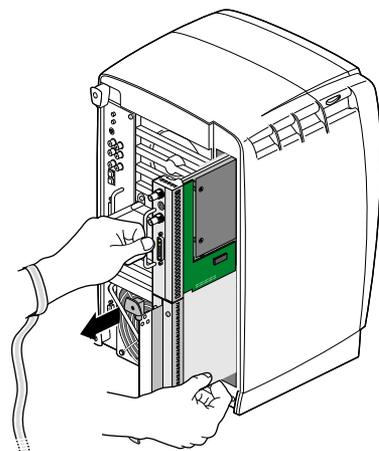


Figure 2-9 Removing the XIO Tri-Module

4. Place the Tri-Module on a flat anti-static surface, such as an empty anti-static bag on your desk.
5. Place a cap on the VPro Graphics Board compression connector.

Spare caps are included with your workstation.

When the XIO Tri-Module is out of the chassis, the sliding handles must protrude, as shown in Figure 2-10. If they do not protrude, pull them out about an inch.

A label identifies each XIO slot (D and A on one side, C and B on the other). Slot B is a daughterboard slot that is located on the other side of the VPro Graphics Board.

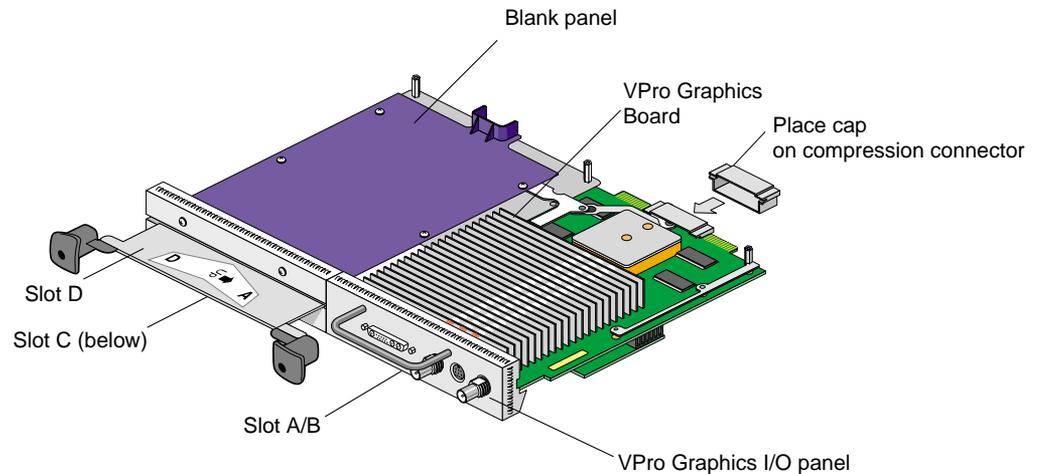


Figure 2-10 XIO Tri-Module

Removing an XIO Option Board or Blank Panel

Before you install an option board in slot C or D, you *must* remove the protective blank panel or the option board currently installed in that slot. To remove an option board or a blank panel, follow these steps:

1. Using the supplied Phillips reversible screwdriver, remove the screws from the option board or blank panel occupying the desired slot, as shown in Figure 2-11.

The following illustrations show you how to remove a blank panel.

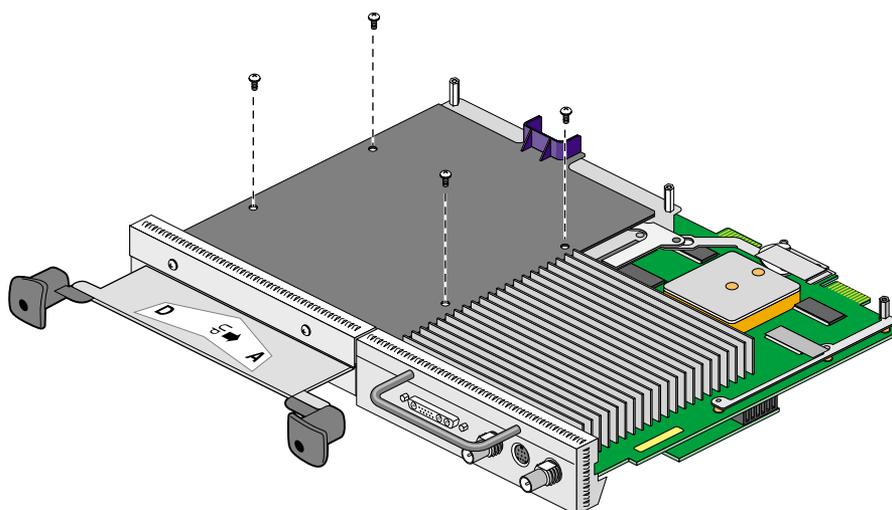


Figure 2-11 Removing the Screws from the Blank Panel

2. Grasp the blank panel or option board on the front and on the side of the board that has no connectors, and lift it, as shown in Figure 2-12.

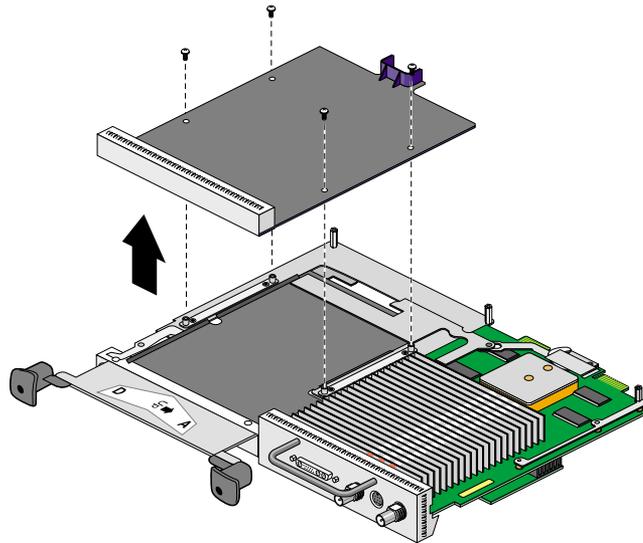


Figure 2-12 Removing the Blank Panel

3. With the same side facing up, place the blank panel or option board on a clean, anti-static surface.

Note: If you removed an option board, store it in an anti-static bag. If you removed a blank panel, store it in a safe place. In the future, if you remove an option board, you need to replace it with another option board or a blank panel.

To reinstall a blank panel, follow the same instructions for installing the DMediaPro board, as described in the next section.

Attaching the DMediaPro Board to the Tri-Module

To attach the DMediaPro Board to the XIO Tri-Module, follow these steps:

1. Remove the DMediaPro Board from its packing.
2. Position the board over the appropriate slot, as shown in Figure 2-13
3. Place the board on the appropriate slot's standoffs, and position the screws.

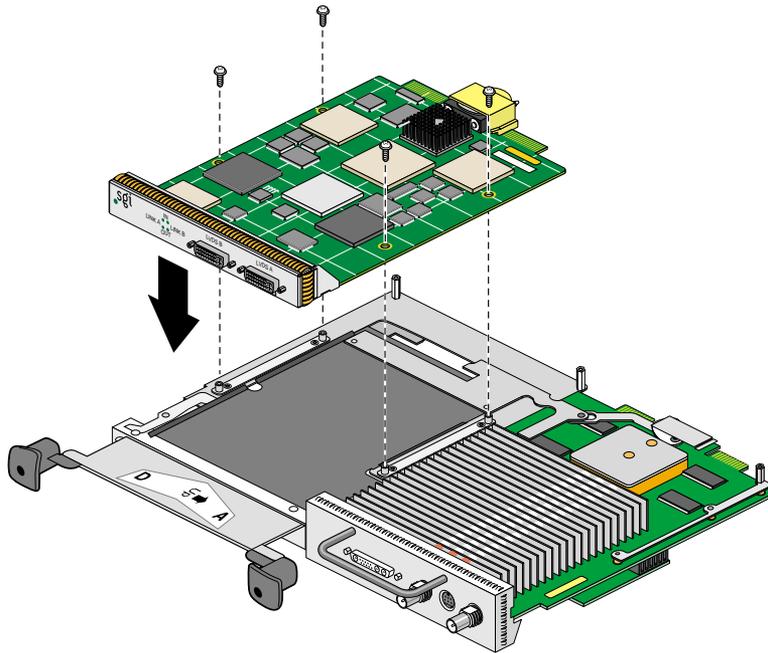


Figure 2-13 Positioning the Board

4. Install the screws, tightening the board to the standoffs, as shown in Figure 2-14.
Make sure all the slots are filled with the VPro Graphics Board, DMediaPro Board, and either an option board or a blank panel. The system does not cool properly if any of the slots are empty.

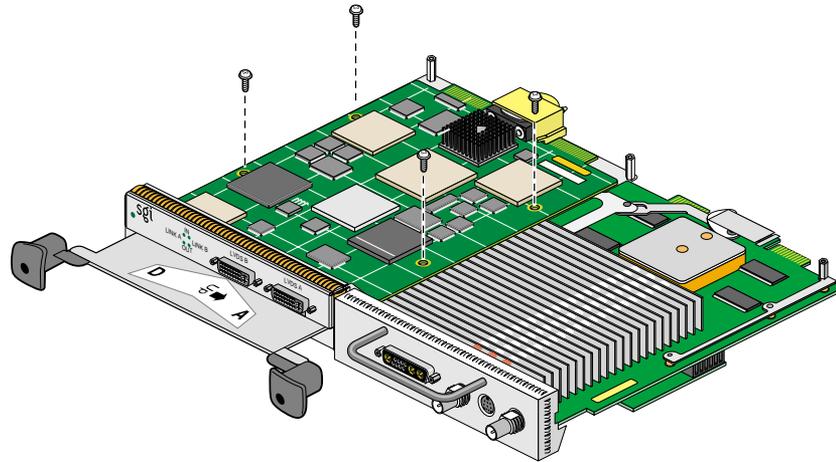


Figure 2-14 Installing the Screws

5. Remove the caps from the XIO compression connectors on the VPro Graphics Board, DMediaPro Board, and any other installed XIO board, as shown in Figure 2-15.
Keep the caps to protect the compression connectors if you remove any XIO boards.

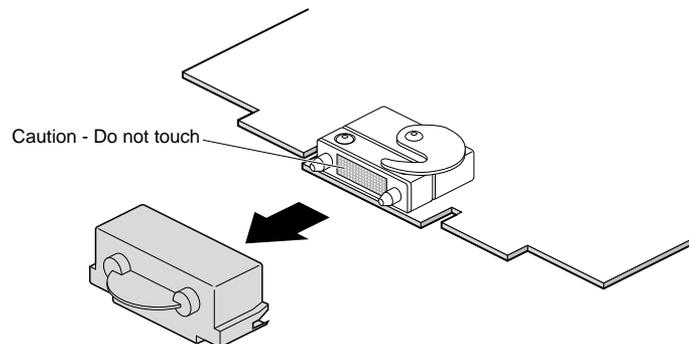


Figure 2-15 Removing the Cap from a Compression Connector

Reinstalling the XIO Tri-Module



Caution: Install the XIO Tri-Module with the VPro Graphics I/O panel aligned with the top of the workstation, as shown in Figure 2-16. The board can be damaged if aligned with the bottom of the workstation.

To reinstall the XIO Tri-Module, follow these steps:

1. Make sure the caps are removed from the compression connectors.
2. Slide the XIO Tri-Module into the guides on the top and bottom of the workstation.
3. Before you insert the XIO Tri-Module, make sure the sliding handles protrude in a locked position from the I/O panels, as shown in Figure 2-16.

If the sliding handles are flush with the I/O panels, the XIO Tri-Module will stop during insertion. Pull out the sliding handles until the sliding portion of the XIO Tri-Module looks like Figure 2-16.

4. Grasp the immovable handle with one hand while supporting the XIO Tri-Module with the other, and slide the module into the chassis.
5. Use the immovable handle to push the XIO Tri-Module into a locked position.
The I/O panels are nearly flush with the workstation when properly inserted, but there is a slight variation in the depth of the boards.
6. Push the sliding handles until the sliding portion of the module is flush with the workstation.

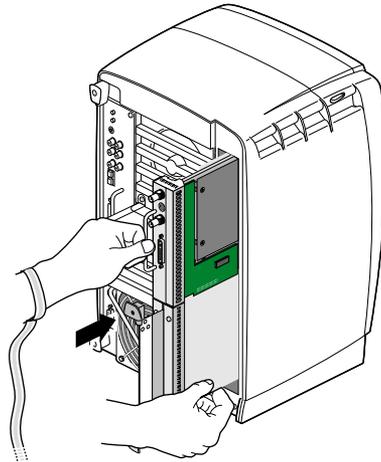


Figure 2-16 Inserting the XIO Tri-Module

7. Tighten the captive screws in the sliding handles, as shown in Figure 2-17.
8. Remove the wrist strap.

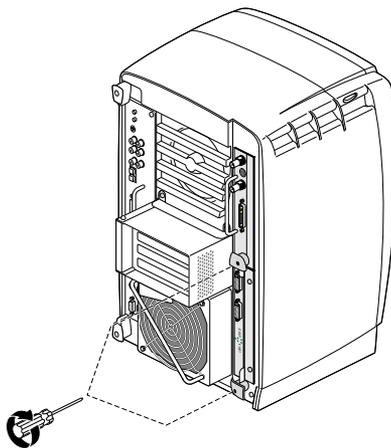


Figure 2-17 Tightening the XIO Tri-Module Captive Screws

9. Reconnect the monitor cable (see Figure 2-18) and all XIO cables to the XIO Tri-Module.

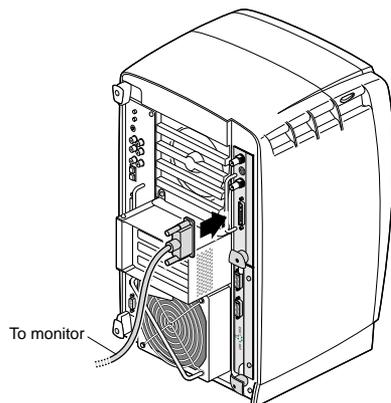


Figure 2-18 Reconnecting the Monitor Cable

Powering On the Workstation

1. Plug the power cable (see A in Figure 2-19) into an electrical outlet.
2. Press the power button (B) on the front of your workstation.
3. Press the monitor power switch (C) to power on your monitor.

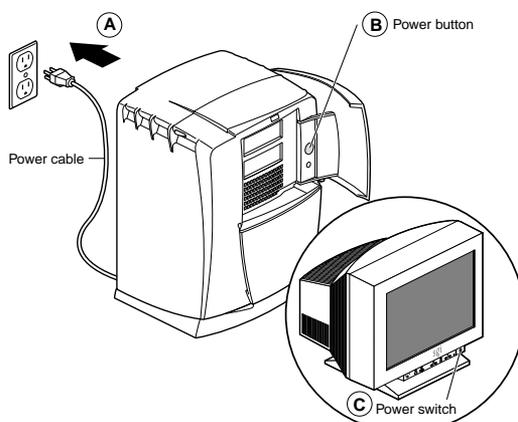


Figure 2-19 Powering On the Workstation

Verifying the Installation

To verify a successful installation of the DMediaPro Board, follow these steps:

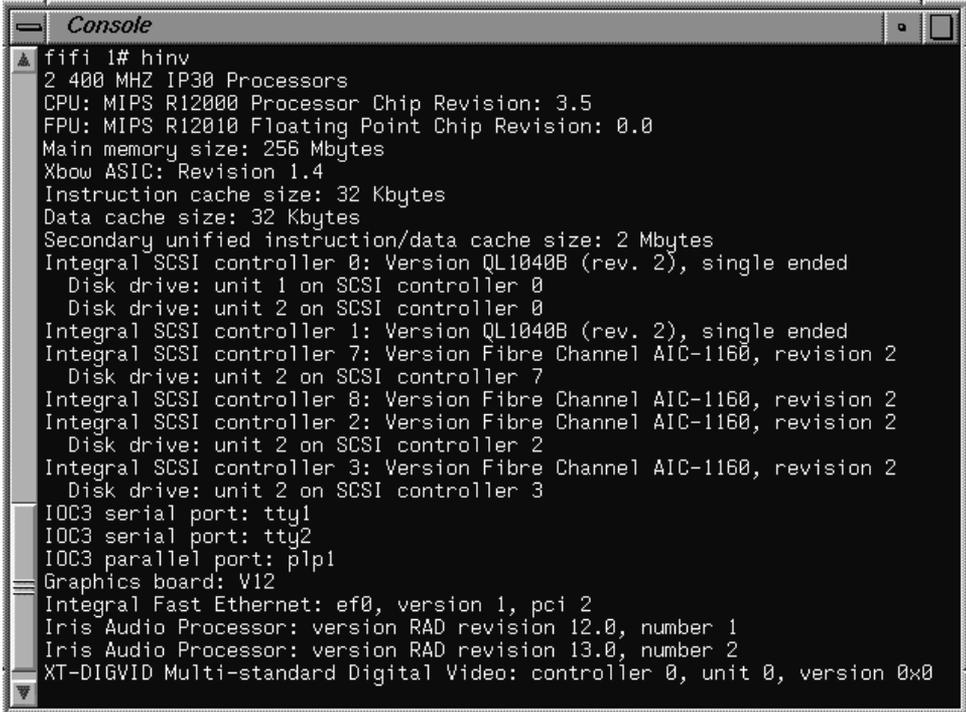
1. Open a UNIX shell.
2. At the prompt, enter `hinv`.

The hardware inventory list appears, as shown in the example in Figure 2-20.

3. Look for the following line near the bottom of the list, which describes the DMediaPro Board.

XT-DIGVID Multi-standard Digital Video: controller 0, unit 0, version 0x0

If the above line does not appear, repeat the installation instructions. If it does not appear after repeating the installation instructions, contact SGI Technical Support.



```

fifi 1# hinv
2 400 MHZ IP30 Processors
CPU: MIPS R12000 Processor Chip Revision: 3.5
FPU: MIPS R12010 Floating Point Chip Revision: 0.0
Main memory size: 256 Mbytes
Xbow ASIC: Revision 1.4
Instruction cache size: 32 Kbytes
Data cache size: 32 Kbytes
Secondary unified instruction/data cache size: 2 Mbytes
Integral SCSI controller 0: Version QL1040B (rev. 2), single ended
  Disk drive: unit 1 on SCSI controller 0
  Disk drive: unit 2 on SCSI controller 0
Integral SCSI controller 1: Version QL1040B (rev. 2), single ended
Integral SCSI controller 7: Version Fibre Channel AIC-1160, revision 2
  Disk drive: unit 2 on SCSI controller 7
Integral SCSI controller 8: Version Fibre Channel AIC-1160, revision 2
Integral SCSI controller 2: Version Fibre Channel AIC-1160, revision 2
  Disk drive: unit 2 on SCSI controller 2
Integral SCSI controller 3: Version Fibre Channel AIC-1160, revision 2
  Disk drive: unit 2 on SCSI controller 3
IOC3 serial port: tty1
IOC3 serial port: tty2
IOC3 parallel port: plp1
Graphics board: V12
Integral Fast Ethernet: ef0, version 1, pci 2
Iris Audio Processor: version RAD revision 12.0, number 1
Iris Audio Processor: version RAD revision 13.0, number 2
XT-DIGVID Multi-standard Digital Video: controller 0, unit 0, version 0x0

```

Figure 2-20 Hardware Inventory List

Connecting the DMediaPro Board to VBOB

This chapter shows you how to connect the DMediaPro Board to VBOB for all High Definition video, Standard Definition video, and Genlock input/output (I/O). The DMediaPro/VBOB configuration allows you to transmit and receive uncompressed High Definition video and Standard Definition video without using two separate connections.

Note: For detailed information on VBOB, see the *SGI Video Breakout Box Owner's Guide*.

The following topics are covered:

- “Getting Started” on page 29
- “Connecting the DMediaPro Board to VBOB” on page 30
- “Setting Up VBOB for High Definition/Standard Definition I/O” on page 31
- “Precautions on SGI Onyx/Origin Systems” on page 32

Getting Started

Before you connect any cables, follow these steps:

1. Power down the SGI host system.
2. Be sure the VBOB power switch at the back of the chassis is in the **Off (o)** position.
3. Connect one end of the VBOB power cord to the VBOB power plug and the other end of the cord to your AC power source.

Connecting the DMediaPro Board to VBOB

To connect the DMediaPro Board to VBOB, follow these steps:

1. Connect one end of the LVDS A cable (black cable with white connector on each end) to the DMediaPro Board's LVDS A connector. Connect the other end of this cable to the VBOB LVDS A connector, as shown in Figure 3-1.
2. Connect one end of the LVDS B cable (black cable with black connector on each end) to the DMediaPro Board's LVDS B connector. Connect the other end of this cable to the VBOB LVDS B connector.

Note: The length of the LVDS cables may affect/restrict hardware positions.

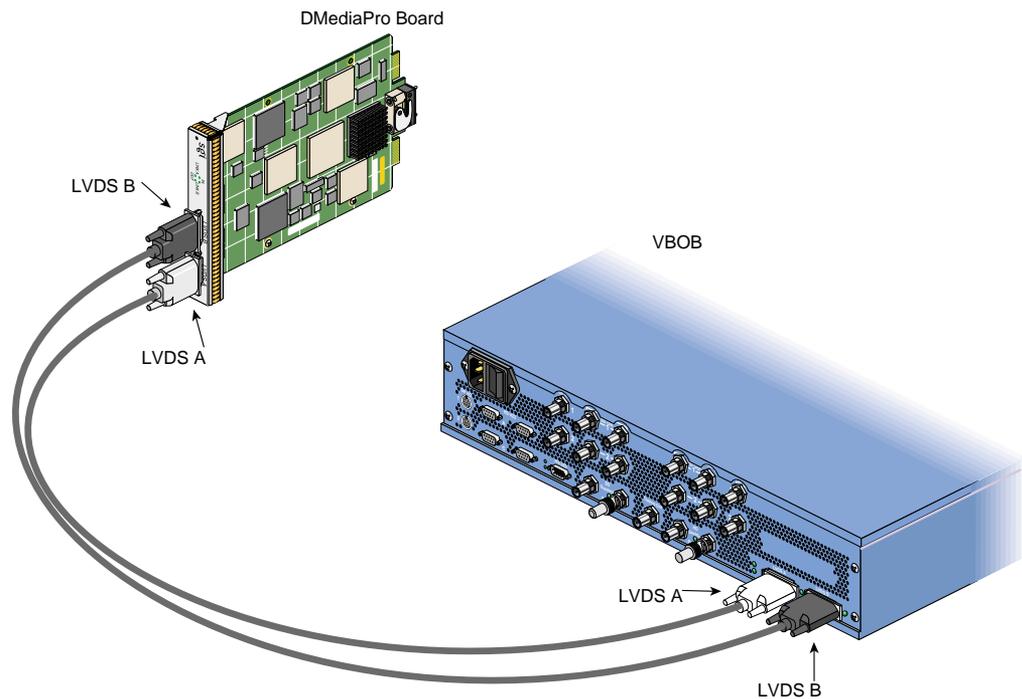


Figure 3-1 Connecting the DMediaPro Board to VBOB

Setting Up VBOB for High Definition/Standard Definition I/O

After you complete the connections in Figure 3-1, you can connect the required cables from the VBOB HD In/Out or SD In/Out connector(s) to the desired High Definition or Standard Definition video device(s). If you are genlocking the serial digital output to an external source, connect an analog sync source to the VBOB HD Genlock In or SD Genlock In connector (see Figure 3-2).

If you are not using High Definition or Standard Definition Genlock loop-throughs, attach a 75 ohm terminator to the appropriate connectors.

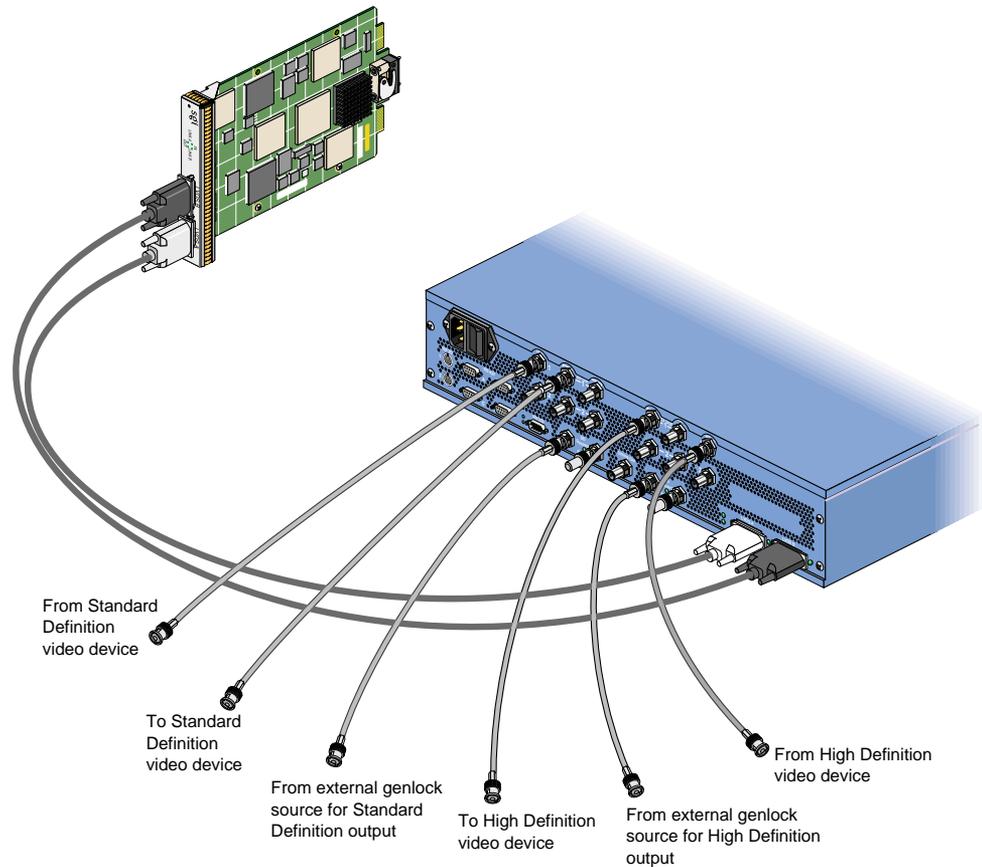


Figure 3-2 Connecting the I/O Cables to VBOB

After you connect the required cables, follow these steps:

1. Turn the VBOB power switch to the **On (-)** position.
2. Boot the SGI host system.

Precautions on SGI Onyx/Origin Systems

- To ensure proper airflow and hardware cooling, ensure that the cables do not hang freely from the VBOB or any bricks/modules. Instead, route the cables through the cable management hardware on the sides of the rack.
- To ensure proper airflow and hardware cooling, the system doors must be closed during normal operation.

Setting Up Audio Synchronization

This chapter shows you how to synchronize audio with video when you use the DMediaPro Board in a typical studio configuration with a tape deck.

The following topics are covered:

- “Synchronizing Audio on an Octane2 Workstation” on page 33
- “Synchronizing Audio on Onyx and Origin Systems” on page 35
- “Setting Up the Audio Panel” on page 37

These configurations allow sample accurate audio/audio and audio/video synchronization.

Synchronizing Audio on an Octane2 Workstation

To synchronize audio on a Silicon Graphics Octane2 V10 or V12 workstation, follow these steps:

1. Connect a house sync generator to a digital tape deck, as shown in Figure 4-1.
2. Connect the AES 1/2 output on the digital tape deck to the coaxial digital input (internal audio) on the rear panel of the Octane2.

This locks the internal audio on the Octane2 to the house sync generator.

For optimized performance and additional functionality, you can purchase the optional SGI PCI Digital Audio Board and install it in the optional PCI module’s half-size slot on the Octane2 rear panel. You can install this half-size board in any of the slots in the PCI module, but you may need to use the two full-size slots in the module for additional requirements, such as fiber channel boards.

Note: For instructions on installing/removing the optional PCI module and PCI option boards, such as the Digital Audio Board, see your *Octane or Octane2 Workstation Owner's Guide*, *Octane PCI Module Installation Guide*, and *SGI PCI Digital Audio Board Installation Guide*.

If you install the optional PCI Digital Audio Board, proceed as follows:

- Connect the provided breakout cable to the DB15 connector on the board.
- Connect the AES 3/4 output on the digital tape deck to the breakout cable's AES input connector (red wire).

For more information on the PCI Digital Audio Board and breakout cable, see the *SGI PCI Digital Audio Board Installation Guide*.

Note: For the optional AES 3/4 configuration, you must use the latest revision of the PCI Digital Audio Board (PN 030-1649-001 or later).

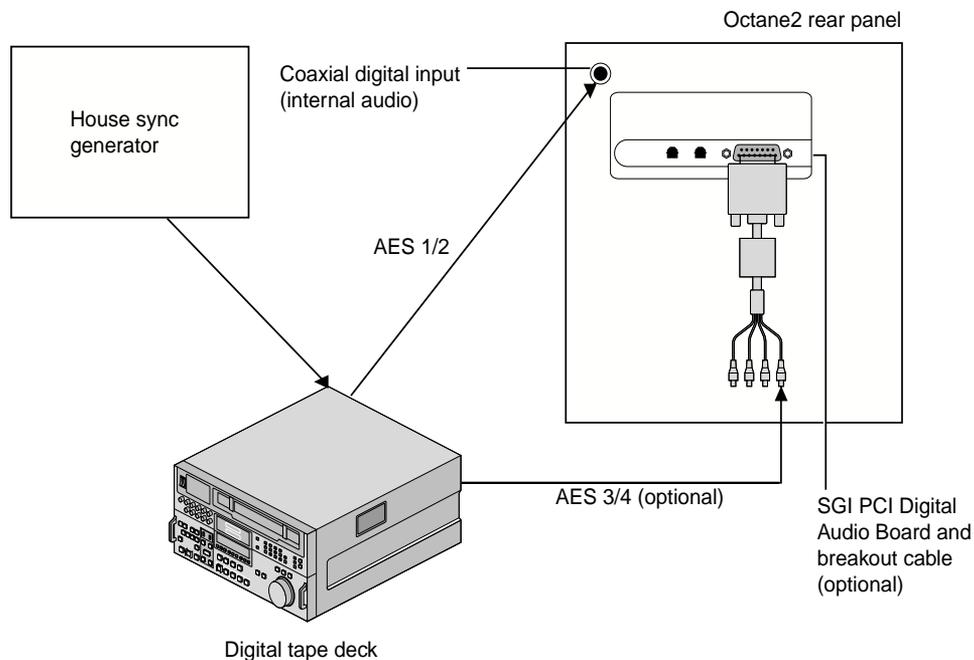


Figure 4-1 Synchronizing Audio on an Octane2 Workstation

Synchronizing Audio on Onyx and Origin Systems

To synchronize audio on SGI Onyx and Origin systems, you need an SGI PCI Digital Audio Board.

Note: The PCI Digital Audio Board is standard equipment on the SGI Onyx 3000 I-Brick. To synchronize audio on an SGI Origin 3000, you must purchase the board and install it in the I-Brick or the optional P-Brick. For the SGI Onyx2 and Origin 2000 systems (when compatible with DMediaPro), the board is optional and *must* be installed by an SGI field installer.



Warning: To prevent serious physical damage in Onyx and Origin systems, you must use the latest revision of the PCI Digital Audio Board (PN 030-1649-001 or later).

To synchronize audio on SGI Onyx and Origin systems, follow these steps:

1. Connect a house sync generator to a digital tape deck, as shown in Figure 4-2.
2. Connect the breakout cable that is included with the PCI Digital Audio Board to the DB15 connector on the board.
3. Connect the AES 1/2 output on the digital tape deck to the PCI Digital Audio Board breakout cable's AES input connector (red wire).

For additional functionality, you can purchase a second PCI Digital Audio Board for your system. A second board is an option for all applicable SGI Onyx and Origin systems.

Note: For instructions on installing PCI boards, such as the Digital Audio Board, see your system owner's guide (Onyx 3000 and Origin 3000 only).

If you have a second PCI Digital Audio Board installed, proceed as follows:

- Connect the provided breakout cable to the DB15 connector on the second board.
- Connect the AES 3/4 output on the digital tape deck to the breakout cable's AES input connector (red wire) on the second board (see Figure 4-2).

For more information on the PCI Digital Audio Board and breakout cable, see the *SGI PCI Digital Audio Board Installation Guide*.

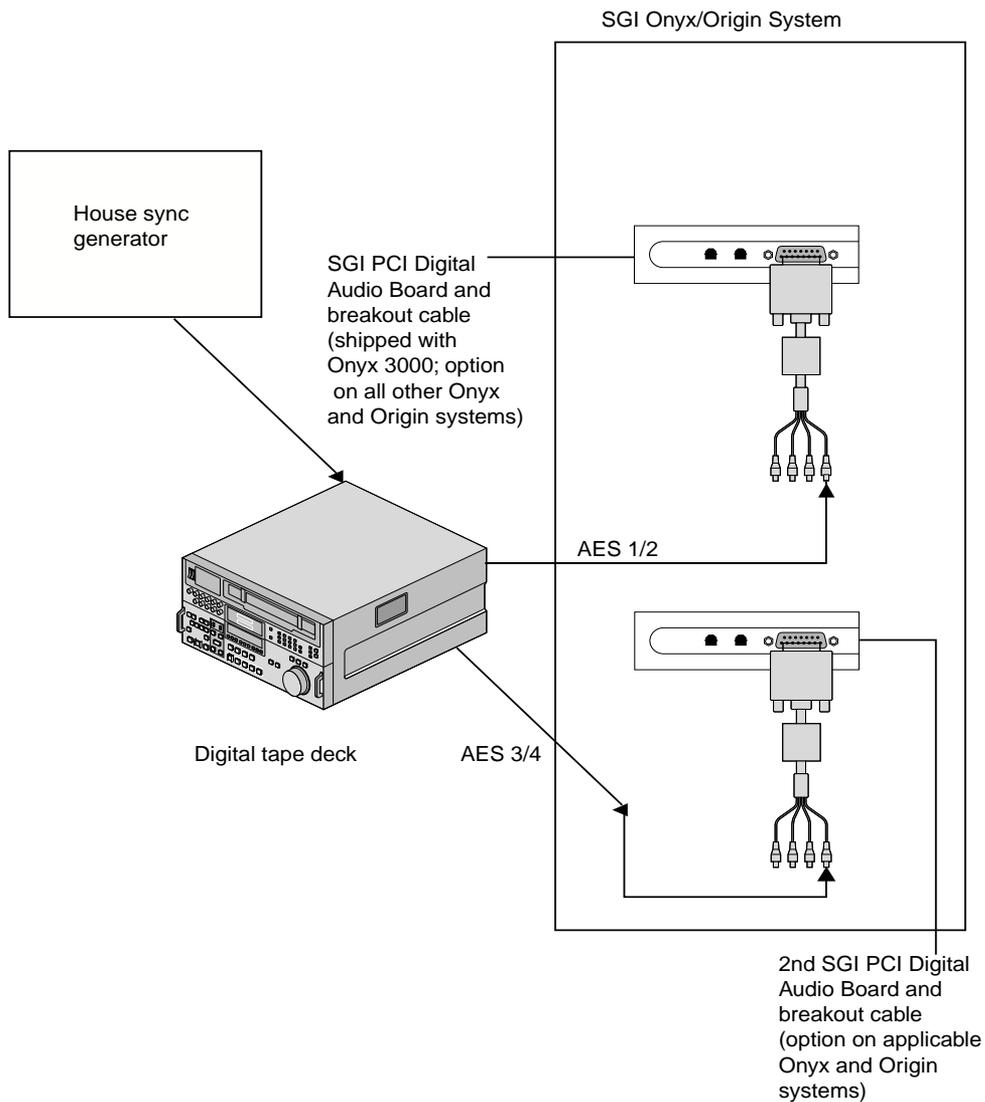


Figure 4-2 Synchronizing Audio on Onyx and Origin Systems

Setting Up the Audio Panel

For the configurations shown on the previous pages, you can use the Audio Panel to display the AES device controls, set the default input and output to AES I/O, set the audio signal path to AES I/O, and set the output sync source.

Displaying AES Device Controls

To display the AES device controls, follow these steps:

1. Open the Audio Panel.
2. From the Toolchest, select Desktop > Control Audio.
3. Select the desired AES device control panel from the View menu.

The selected device control panel appears, where you can adjust parameters such as sample rate, input source, and output destination. For details, refer to the Audio Panel Help menu.

Setting the Default Input and Output to AES

The Audio Panel displays device controls for ADAT In, ADAT Out, AES In, and AES Out for each PCI Digital Audio Board installed in your system. You can designate any of these devices as a default, which means your system uses the device as the internal audio device unless otherwise specified by another application. To set the default input and output, simply open the Audio Panel and select a default input and output device in the Default menu.

Setting the Input and Output Signal Path

You can select either electrical or optical signal paths for the AES input and output devices. To set the input source with the Audio Panel, follow these steps:

1. Position the cursor over the input device panel (if the device panel you need is not displayed, use the View menu), then hold down the right mouse button to display the menu for the desired input device.
2. Select Preferences in the input device menu.

The Preferences menu appears for the respective input device.

3. Choose the input source (for example, AES In) that you want the input device to use. "AES In" is the electrical input.

To set the output destination with the Audio Panel, follow these steps:

1. Position the cursor over the output device panel (if the device panel you need is not displayed, use the View menu), then hold down the right mouse button to display the menu for the desired output device.
2. Select Preferences in the output device menu, as shown in Figure 4-3.

The Preferences menu appears for the respective output device, as shown in Figure 4-4.

3. Choose the output destination (for example, "AES Out") that you want the output device to use. "AES Out" is the coaxial digital electrical output.

Selecting the optical input or output for AES disables the ADAT input or output, because the two devices share the same optical connector. Similarly, selecting the optical input or output for ADAT automatically switches the AES input or output to the coaxial digital electrical connector.

If more than one PCI Digital Audio Board is installed, the system names each board using an incremental prefix naming scheme. For this type of configuration, one AES input is displayed as "RAD 1.AES In" and the other as "RAD 2.AES In." Also, one AES output is displayed as "RAD 1.AES Out" and the other as "RAD 2.AES Out" (see Figure 4-3).

Setting the Output Sync Source

To set the output sync source, follow these steps:

1. Position the cursor over the output device panel (if the device panel you need is not displayed, use the View menu), then hold down the right mouse button to display the menu for the desired output device.
2. Select Preferences in the output device menu, as shown in Figure 4-3.

The Preferences menu appears for the respective output device, as shown in Figure 4-4.

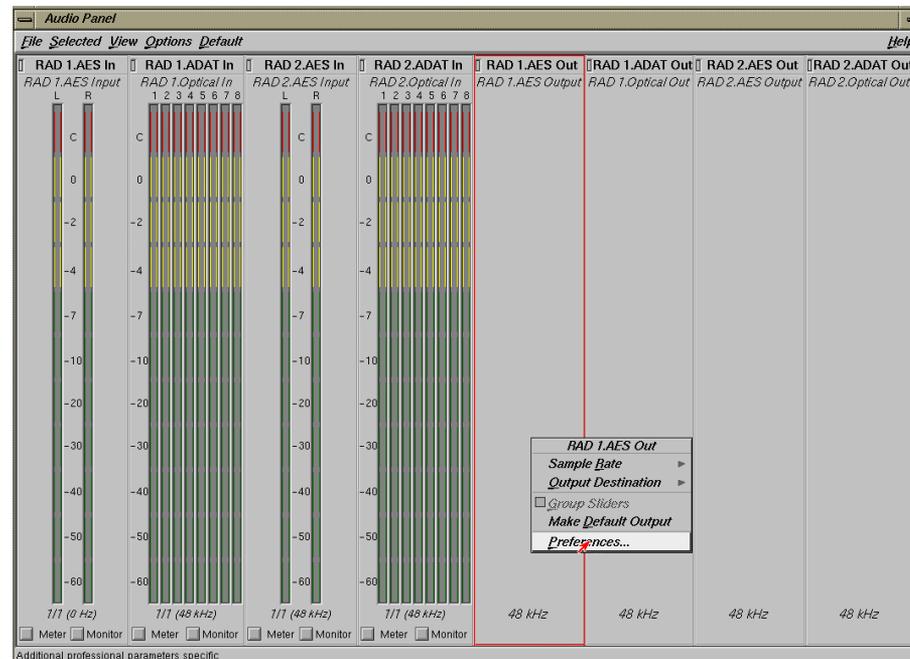


Figure 4-3 Selecting Preferences for the Output Device

- Choose the sync source that you want the output device to use.

The example in Figure 4-4 shows how to set up the configuration displayed in Figure 4-1 for synchronizing the Octane2 internal audio using the AES input.

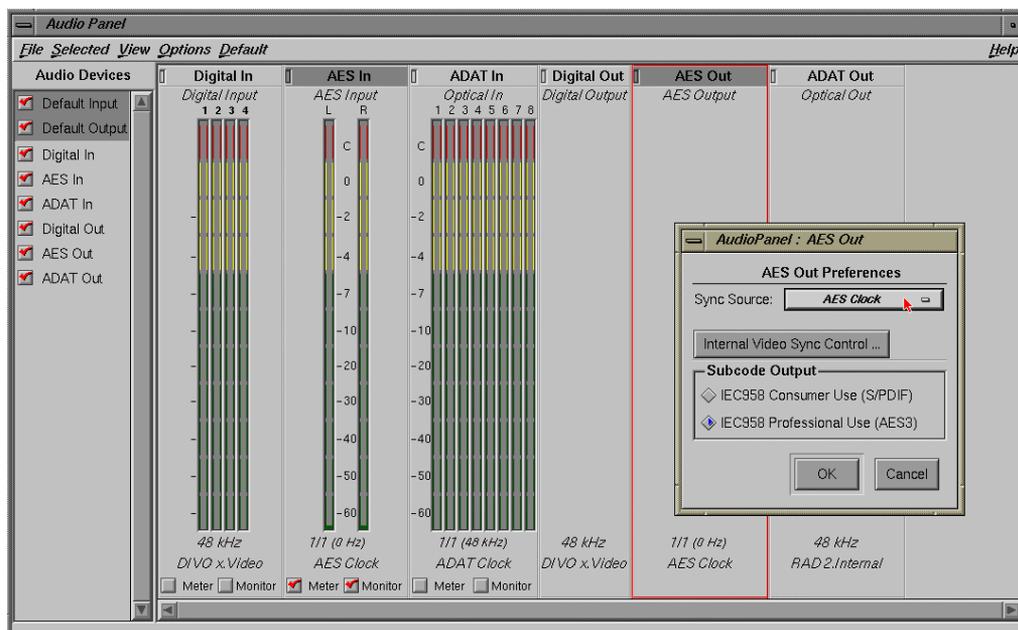


Figure 4-4 Synchronizing the Octane2 Internal Audio

The example in Figure 4-5 shows how to set up the single board configuration shown in Figure 4-2 for an Onyx or Origin system.

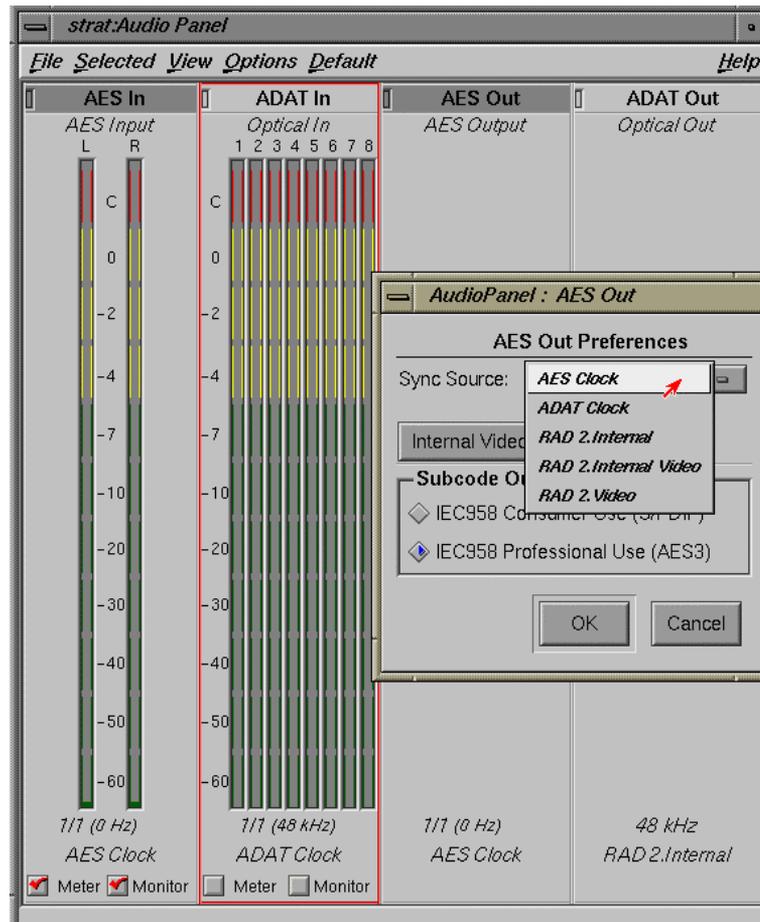


Figure 4-5 Synchronizing a Single PCI Digital Audio Board on an Onyx or Origin System

The example in Figure 4-6 shows how to set up the RAD 1.AES Out Preferences for the two-board configuration (Figure 4-2) on an Onyx or Origin system.

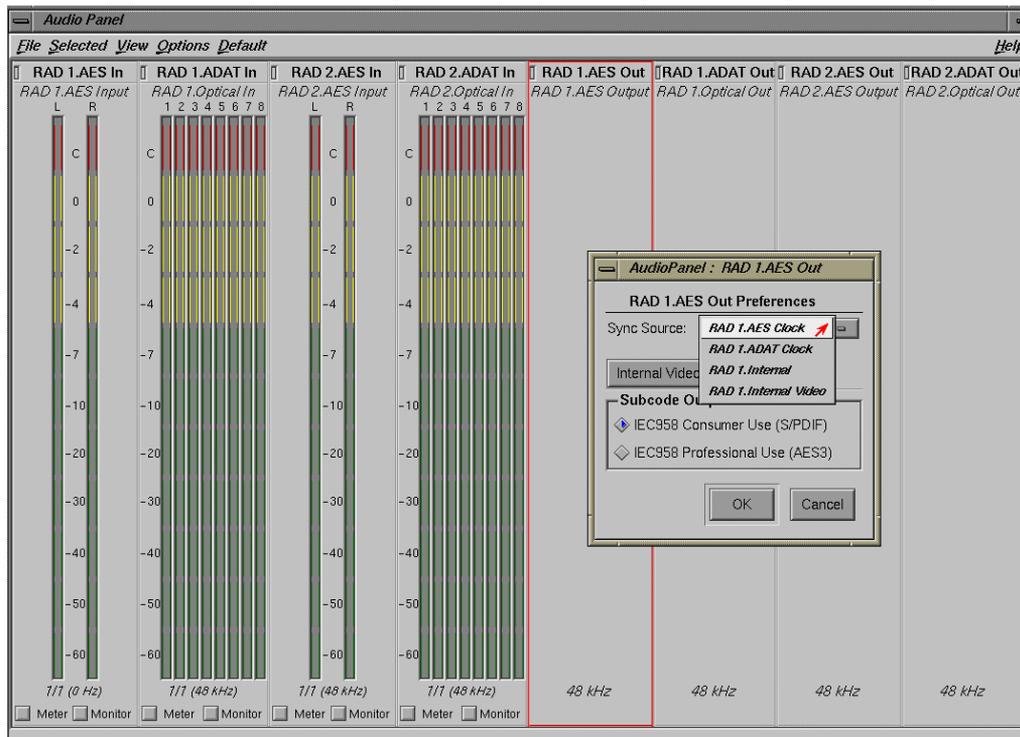


Figure 4-6 Synchronizing Two PCI Digital Audio Boards on an Onyx/Origin System (RAD 1.AES Out Preferences)

The example in Figure 4-7 shows how to set up the RAD 2.AES Out Preferences for the two-board configuration (Figure 4-2) on an Onyx or Origin system.

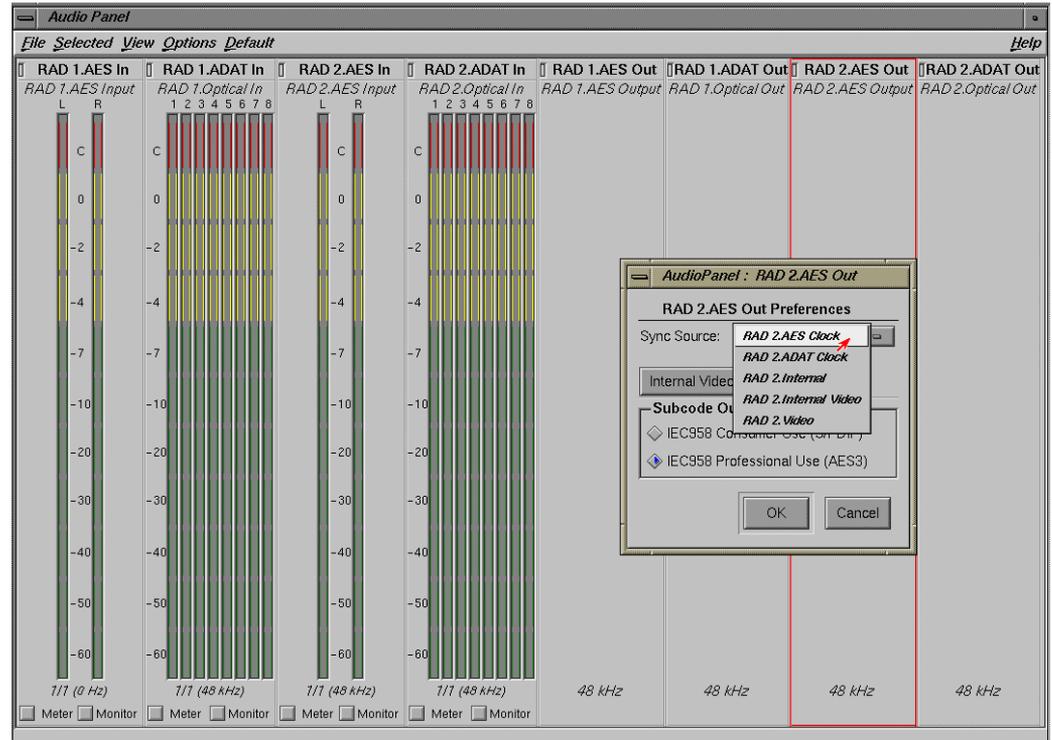


Figure 4-7 Synchronizing Two PCI Digital Audio Boards on an Onyx/Origin System (RAD 2.AES Out Preferences)

Other Configurations

The DMediaPro Board does not support audio synchronization using “Internal Video” as a “Sync Source” in the Audio Panel AES or ADAT “Out Preferences” or the Analog “In/Out Preferences.”

In addition to the examples described earlier in this chapter, there are other optional configurations. For example, you can synchronize the PCI Digital Audio Board’s audio input to a house sync generator as follows:

1. Connect the house sync generator to one of the breakout cable’s video reference loop connectors (green or black wires).

If you are not using the other video reference loop connector to loop the video reference signal through another device, place a 75-ohm terminator on the unused connector.

2. Open the Audio Panel, hold down the right mouse button on the desired output device, select **Preferences** in the output device menu, and then select **Video** as the Sync Source.

Note: To synchronize a digital audio (AES or ADAT) input to a video reference, the input must be synchronized externally because it is externally sampled. The examples described earlier in this chapter (using a tape deck) reflect this requirement.

Programming the DMediaPro Board

This chapter provides a DMediaPro Board Programming overview. The DMediaPro Board supports the OpenML Media Library Software Development Kit (ML). This API is described in the *OpenML Media Library Software Development Kit Programmer's Guide* (referred to as the *ML Programmer's Guide* throughout this chapter).

The following topics are covered:

- “Programming Basics for the DMediaPro Board” on page 46
- “DMediaPro Controls” on page 46
- “DMediaPro Events” on page 81
- “Synchronizing Data Streams and Signals” on page 92
- “Restrictions and Important Notes” on page 92

Programming Basics for the DMediaPro Board

After installing the DMediaPro software and the DMediaPro Board, (see Chapter 2), if you want to build programs that run under ML, follow these steps:

1. In your source code, include the following header files:

- `ML/ml.h`
- `ML/mlu.h`
- `ML/ml_xtdigvid.h`

2. Link with `libML` and `libMLU`

You can find several useful MLprogramming examples in `/usr/share/src/ml/video/xtdigvid/examples` on the DMediaPro CD. You can also find some programming examples later in this chapter.

DMediaPro Controls

This section covers the following topics:

- “Path Controls and Jack Controls” on page 47
- “DMediaPro Control Summary” on page 50
- “DMediaPro Default Path Controls” on page 65

Path Controls and Jack Controls

The DMediaPro Board supports two types of controls: path controls and jack controls.

Path Controls

With path controls, you can set up the following types of data transfer paths:

- Memory to video path
- Video to memory path

Using these path controls, you can transfer data from memory to an SD/HD video jack or transfer data from an SD/HD video jack to memory (see Figure 5-1).

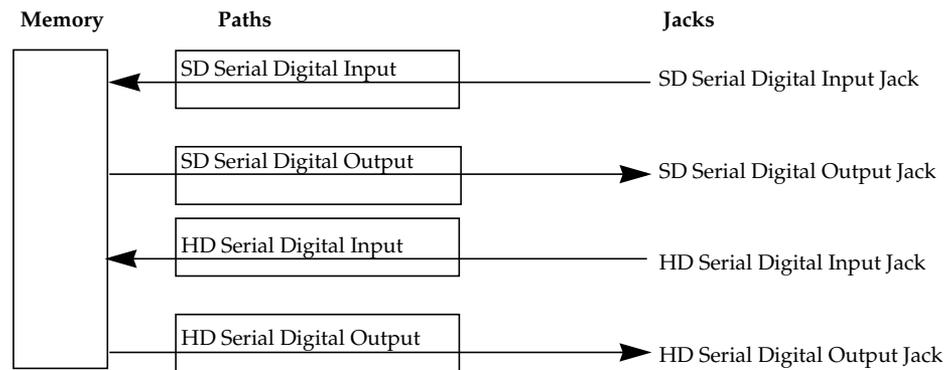


Figure 5-1 Setting Up Paths

Jack Controls

With jack controls you can adjust controls on a jack without setting up a data transfer path.

Using some jack controls, you can adjust certain parameters while a data transfer is in progress. However, you can only use this type of jack control to adjust parameters that do not affect memory to video and video to memory data transfers. For example, you can adjust the EE mode (XTDIGVID_EE_MODE_INT32) during a transfer (see Figure 5-2), but you cannot use jack controls to adjust the colorspace or memory packing order parameters.

Note: When a jack control is adjustable during a transfer, a special access mode is automatically enabled. This access mode overrides the default setting which normally disallows the changing of controls during a transfer.

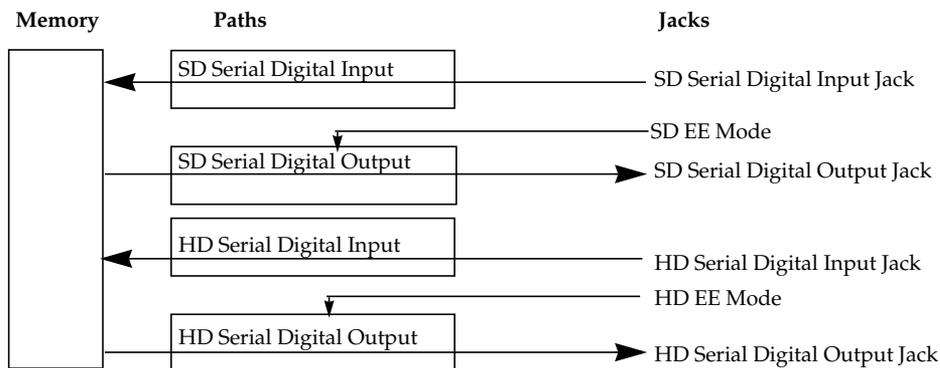


Figure 5-2 Using a Jack Control to Change the EE Mode During a Transfer

Following are the DMediaPro Board jack controls for the HD jacks and the SD jacks.

HD Serial Digital Input Jack

XTDIGVID_LOOPBACK_INT32

HD Serial Digital Output Jack

ML_VIDEO_GENLOCK_SOURCE_TIMING_INT32

ML_VIDEO_GENLOCK_TYPE_INT32

XTDIGVID_EE_MODE_INT32

ML_VIDEO_H_PHASE_INT32

ML_VIDEO_V_PHASE_INT32

SD Serial Digital Input Jack

XTDIGVID_LOOPBACK_INT32

SD Serial Digital Output Jack

ML_VIDEO_GENLOCK_SOURCE_TIMING_INT32

ML_VIDEO_GENLOCK_TYPE_INT32

XTDIGVID_EE_MODE_INT32

ML_VIDEO_H_PHASE_INT32

ML_VIDEO_V_PHASE_INT32

Note: For an example on setting up a jack control, go to “Setting Controls on a Jack” on page 90.

DMediaPro Control Summary

Table 5-1 shows the input/output paths for each of the DMediaPro Board Controls.

Table 5-1 HD/SD Input and Output Paths

Control Parameters	Input Video Path	Input Image Memory Buffer	Output Video Path	Output Image Memory Buffer
ML_IMAGE_BUFFER_POINTER		X		X
ML_IMAGE_WIDTH_INT32		X		X
ML_IMAGE_HEIGHT_1_INT32		X		X
ML_IMAGE_HEIGHT_2_INT32		X		X
ML_IMAGE_PACKING_INT32		X		X
ML_IMAGE_SAMPLING_INT32		X		X
ML_IMAGE_COMPRESSION_INT32		X		X
ML_IMAGE_COLORSPACE_INT32		X		X
ML_IMAGE_ROW_BYTES_INT32		X		X
ML_IMAGE_SKIP_PIXELS_INT32		X		X
ML_IMAGE_SKIP_ROWS_INT32		X		X
ML_IMAGE_ORIENTATION_INT32		X		X
ML_IMAGE_TEMPORAL_SAMPLING_INT32		X		X
ML_IMAGE_INTERLEAVE_MODE_INT32		X		X
ML_IMAGE_DOMINANCE_INT32		X		X
ML_IMAGE_BUFFER_SIZE_INT32		X(Read only)		X(Read only)
ML_VIDEO_UST_INT64	X(Read only)		X(Read only)	
ML_VIDEO_MSC_INT64	X(Read only)		X(Read only)	
ML_VIDEO_TIMING_INT32	X		X	
ML_VIDEO_COLORSPACE_INT32	X		X	
ML_VIDEO_PRECISION_INT32	X		X	

Table 5-1 (continued) HD/SD Input and Output Paths

Control Parameters	Input Video Path	Input Image Memory Buffer	Output Video Path	Output Image Memory Buffer
ML_VIDEO_SAMPLING_INT32	X		X	
ML_VIDEO_START_X_INT32	X		X	
ML_VIDEO_START_Y_F1_INT32	X		X	
ML_VIDEO_START_Y_F2_INT32	X		X	
ML_VIDEO_WIDTH_INT32	X		X	
ML_VIDEO_HEIGHT_F1_INT32	X		X	
ML_VIDEO_HEIGHT_F2_INT32	X		X	
XTDIGVID_LUT_YG_INT32_ARRAY	X		X	
XTDIGVID_LUT_UB_INT32_ARRAY	X		X	
XTDIGVID_LUT_VR_INT32_ARRAY	X		X	
ML_DEVICE_STATE_INT32	X		X	
ML_DEVICE_EVENTS_INT32_ARRAY	X		X	
ML_QUEUE_SEND_COUNT_INT32	X		X	
ML_QUEUE_RECEIVE_COUNT_INT32	X		X	
ML_QUEUE_SEND_WAITABLE_INT32	X		X	
ML_QUEUE_RECEIVE_WAITABLE_INT32	X		X	
ML_VIDEO_GENLOCK_TYPE_INT32			X	
ML_VIDEO_GENLOCK_SOURCE_TIMING_INT32			X	
ML_VIDEO_H_PHASE_INT32			X	
ML_VIDEO_V_PHASE_INT32			X	
ML_VIDEO_OUTPUT_REPEAT_INT32			X	
XTDIGVID_EE_MODE_INT32			X	
XTDIGVID_FF_MODE_INT32			X	

Table 5-1 (continued) HD/SD Input and Output Paths

Control Parameters	Input Video Path	Input Image Memory Buffer	Output Video Path	Output Image Memory Buffer
XTDIGVID_LOOPBACK_INT32	X (Serial input only/not applicable for graphics input)			
ML_VIDEO_GENLOCK_SIGNAL_PRESENT_INT32			X(Read only)	
ML_VIDEO_SIGNAL_PRESENT_INT32	X(Read only)			
XTDIGVID_GENLOCK_STATE_INT32			X(Read only)	
XTDIGVID_GENLOCK_ERROR_STATUS_INT32			X(Read only)	
ML_OPEN_MODE_INT32	X		X	
ML_OPEN_SEND_QUEUE_COUNT_INT32	X		X	
ML_OPEN_RECEIVE_QUEUE_COUNT_INT32	X		X	
ML_OPEN_MESSAGE_PAYLOAD_SIZE_INT32	X		X	
ML_OPEN_EVENT_PAYLOAD_COUNT_INT32	X		X	
ML_OPEN_SEND_SIGNAL_COUNT_INT32	X		X	

Table 5-2 defines the value(s) and use for each of the DMediaPro Board controls. For a detailed description of the ML_ controls, see the *ML Programmer's Guide*. You can find more information on the device-specific (XTDIGVID_) controls later in this guide.

Table 5-2 DMediaPro Board Control Parameters/Value(s) and Use

Control Parameters	Range or Value(s)	Use
ML_IMAGE_BUFFER_POINTER	N/A	Pointer to the first byte of an image buffer in memory. The buffer address must comply with the alignment constraints for buffers on the specific path or transcoder to which it is being sent.
ML_IMAGE_WIDTH_INT32	Defined by selected timing.	Defines image width. Must be the same as ML_VIDEO_WIDTH_INT32.
ML_IMAGE_HEIGHT_1_INT32	Number of lines in the frame for progressive or interleaved images. Number of lines in the first field for non-interleaved images.	Defines the height of F1 field in lines. Must be set to full image height for progressive formats or when ML_INTERLEAVE_MODE_INT32 is set to ML_INTERLEAVE_MODE_INTERLEAVED.
ML_IMAGE_HEIGHT_2_INT32	Number of lines in the second field of a non-interleaved image (must be set to zero for progressive and interleaved modes).	Defines the height of F2 field in lines. Set to zero for progressive formats or when ML_INTERLEAVE_MODE_INT32 is set to ML_INTERLEAVE_MODE_INTERLEAVED.

Table 5-2 (continued) DMediaPro Board Control Parameters/Value(s) and Use

Control Parameters	Range or Value(s)	Use
ML_IMAGE_PACKING_INT32	ML_PACKING_8 ML_PACKING_8_R ML_PACKING_8_3214 ML_PACKING_10 ML_PACKING_10_3214 ML_PACKING_10in16L ML_PACKING_10in16L_3214 ML_PACKING_10in16R ML_PACKING_10in16R_3214 ML_PACKING_S12in16L ML_PACKING_S12in16R ML_PACKING_10_10_10_2 ML_PACKING_10_10_10_2_R ML_PACKING_10_10_10_2_3214	Describes the packing format of data in memory as follows: <i>ML_PACKING_type_size_order</i> <i>type</i> is the base type of each component. Leave blank for an unsigned integer. Use S for a signed integer (in a future release, ML may also support R for real numbers). <i>size</i> defines the number of bits per component. The size may refer to simple, padded, or complex packings. <i>order</i> is the order of the components in memory. Leave blank for natural ordering (1,2,3,4). Use R for reversed ordering (4,3,2,1). For all other orderings, specify the component order explicitly. See the <i>ML Programmer's Guide</i> for more detailed information.
ML_IMAGE_SAMPLING_INT32	ML_SAMPLING_422 (CbYCr only) ML_SAMPLING_4224 (CbYCr only) ML_SAMPLING_444 (CbYCr and RGB) ML_SAMPLING_4444 (CbYCr and RGB)	Specifies how often each component is sampled for each pixel.
ML_IMAGE_COMPRESSION_INT32	ML_COMPRESSION_UNCOMPRESSED	Describes the desired compression factor. The size of the uncompressed buffer depends on image width, height, packing, and sampling. The default value is implementation-dependent, but should represent a reasonable trade-off between compression time, quality, and bandwidth.

Table 5-2 (continued) DMediaPro Board Control Parameters/Value(s) and Use

Control Parameters	Range or Value(s)	Use
ML_IMAGE_COLORSPACE_INT32	ML_COLORSPACE_RGB_601_FULL ML_COLORSPACE_CbYCr_601_HEAD ML_COLORSPACE_CbYCr_601_FULL ML_COLORSPACE_RGB_601_HEAD ML_COLORSPACE_CbYCr_709_HEAD ML_COLORSPACE_CbYCr_709_FULL ML_COLORSPACE_RGB_709_HEAD ML_COLORSPACE_RGB_709_FULL ML_COLORSPACE_CbYCr_240M_HEAD ML_COLORSPACE_CbYCr_240M_FULL ML_COLORSPACE_RGB_240M_HEAD ML_COLORSPACE_RGB_240M_FULL	Specifies the colorspace of image data in memory as follows: ML_COLORSPACE_ <i>representation_standard_range</i> where: <i>representation</i> controls how to interpret each component. <i>standard</i> indicates how to interpret particular values as actual colors. <i>range</i> is either ML_RANGE_FULL, where the smallest and largest values are limited only by the available packing size, or ML_RANGE_HEAD, where the smallest and largest values are somewhat less than the theoretical min/max values to allow some "headroom."
ML_IMAGE_ROW_BYTES_INT32	[0 - 0]	Number of bytes along one row of the image memory buffer. If this value is 0, each row is exactly IMAGE_WIDTH * pixels wide. Default is 0. For more information, see the <i>ML Programmer's Guide</i> .
ML_IMAGE_SKIP_PIXELS_INT32	[0 - 0]	Number of pixels to skip at the start of each row in the image memory buffer. Default is 0. Must be 0 if ROW_BYTES is 0. Default is 0.
ML_IMAGE_SKIP_ROWS_INT32	[0 - 0]	Number of rows to skip at the start of each image memory buffer. Default is 0.
ML_IMAGE_ORIENTATION_INT32	ML_ORIENTATION_TOP_TO_BOTTOM ML_ORIENTATION_BOTTOM_TO_TOP	Sets the orientation of the image in either natural video order or natural graphics order. ML_ORIENTATION_TOP_TO_BOTTOM sets the image in natural video order - pixel [0,0] is at the top left of the image. ML_ORIENTATION_BOTTOM_TO_TOP sets the image in natural graphics order - pixel [0,0] is at the bottom left of the image.

Table 5-2 (continued) DMediaPro Board Control Parameters/Value(s) and Use

Control Parameters	Range or Value(s)	Use
ML_IMAGE_TEMPORAL_SAMPLING_INT32	ML_TEMPORAL_SAMPLING_FIELD_BASED ML_TEMPORAL_SAMPLING_PROGRESSIVE	Specifies whether the image temporal sampling is progressive or interlaced.
ML_IMAGE_INTERLEAVE_MODE_INT32	ML_INTERLEAVE_MODE_INTERLEAVED ML_INTERLEAVE_MODE_SINGLE_FIELD	Only used for interlaced images. This parameter specifies whether the two fields are interleaved into a single image (and reside in a single buffer) or are stored in two separate fields (therefore, in two separate buffers). This parameter is ignored for signals with progressive timing.
ML_IMAGE_DOMINANCE_INT32	ML_DOMINANCE_F1 (default) ML_DOMINANCE_F2	Identifies frame boundaries in a field sequence (interlaced formats).
ML_IMAGE_BUFFER_SIZE_INT32	The size of the image buffer in bytes.	To obtain the size of the image buffer in bytes. This read only parameter is computed using the current path control settings. This value represents the worst-case buffer size.
ML_VIDEO_UST_INT64	Value of UST at the time the data begins to move through the jack.	The unadjusted system time (UST) is the timestamp that corresponds to the time when the data begins to move through the jack. For video, this corresponds to the beginning of a vertical sync. This parameter can be sent to a video path along with a buffer, using the dmSendBuffers call.
ML_VIDEO_MSC_INT64	Value of MSC at the time the data begins to move through the jack	The media stream count (MSC) is the timestamp that corresponds to the time when the data begins to move through the jack. For video, this corresponds to the beginning of a vertical sync. This parameter can be sent to a video path along with a buffer, using the dmSendBuffers call.

Table 5-2 (continued) DMediaPro Board Control Parameters/Value(s) and Use

Control Parameters	Range or Value(s)	Use
ML_VIDEO_TIMING_INT32	ML_TIMING_1125_1920x1080_60i ML_TIMING_1125_1920x1080_5994i ML_TIMING_750_1280x720_60p ML_TIMING_750_1280x720_5994p ML_TIMING_1125_1920x1080_50i ML_TIMING_1125_1920x1080_25p ML_TIMING_1125_1920x1080_24p ML_TIMING_1125_1920x1080_2398p ML_TIMING_1125_1920x1035_5994i ML_TIMING_1125_1920x1080_24PsF ML_TIMING_1125_1920x1080_2398PsF ML_TIMING_1125_1920x1080_25PsF ML_TIMING_525 ML_TIMING_625	Sets the timing on an input or output video path. Not all timings are supported on all devices. On devices that can auto-detect, the timing can be read-only on input.
ML_VIDEO_COLORSPACE_INT32	ML_COLORSPACE_CbYCr_601_HEAD ML_COLORSPACE_RGB_601_HEAD ML_COLORSPACE_CbYCr_709_HEAD ML_COLORSPACE_RGBr_709_HEAD ML_COLORSPACE_CbYCr_240M_HEAD ML_COLORSPACE_RGB_240M_HEAD	Specifies the colorspace of the video data on the video jack. For input paths, this is the colorspace you expect to receive at the jack. For output paths, it is the colorspace you desire at the jack.
ML_VIDEO_PRECISION_INT32	[8 - 8], [10 - 10]	Specifies whether the external video interface is 8 bits or 10 bits wide. This is the precision (number of bits of resolution) of the signal at the jack. This is an integer. A precision value of 10 specifies a 10-bit signal. A value of 8 specifies an 8-bit signal.
ML_VIDEO_SAMPLING_INT32	ML_SAMPLING_422 ML_SAMPLING_4224 ML_SAMPLING_444 ML_SAMPLING_4444	Specifies the sampling of video data on the video jack.
ML_VIDEO_START_X_INT32	[1 - 1]	Sets the start horizontal location on each line of the video signal.

Table 5-2 (continued) DMediaPro Board Control Parameters/Value(s) and Use

Control Parameters	Range or Value(s)	Use
ML_VIDEO_START_Y_F1_INT32	Defined by selected timing.	Sets the start vertical location on F1 fields of the video signal. For progressive signals, this parameter specifies the start of every frame.
ML_VIDEO_START_Y_F2_INT32	Defined by selected timing.	Sets the start vertical location on F2 fields of the video signal. This parameter is ignored for progressive timing signals.
ML_VIDEO_WIDTH_INT32	Defined by selected timing.	Defines video width. This must be the same as ML_IMAGE_WIDTH_INT32. Sets the horizontal width of the clipping region on each line of the video signal.
ML_VIDEO_HEIGHT_F1_INT32	Number of lines in the frame for progressive formats. Number of lines in the first field for interlaced or progressive segmented frames (PsF) formats.	Defines the height of F1 field in lines. Must be set to full image height for progressive formats.
ML_VIDEO_HEIGHT_F2_INT32	Number of lines in the second field for interlaced or PsF formats.	Defines the height of F2 field in lines. For progressive signals, this value must be 0.
XTDIGVID_LUT_YG_INT32_ARRAY	Integer for YG LUT values.	Defines the LUT values for the YG LUT.
XTDIGVID_LUT_UB_INT32_ARRAY	Integer for UB LUT values.	Defines the LUT values for the UB LUT.
XTDIGVID_LUT_VR_INT32_ARRAY	Integer for VR LUT values.	Defines the LUT values for the VR LUT.
ML_DEVICE_STATE_INT32	ML_DEVICE_STATE_TRANSFERRING ML_DEVICE_STATE_WAITING ML_DEVICE_STATE_ABORTING ML_DEVICE_STATE_FINISHING ML_DEVICE_STATE_READY	Defines how the device transitions through well-known states. The device state can be changed with dmBeginTransfer() and dmEndTransfer().
ML_DEVICE_EVENTS_INT32_ARRAY	ML_EVENT_VIDEO_SEQUENCE_LOST ML_EVENT_VIDEO_SYNC_LOST ML_EVENT_VIDEO_SYNC_GAINED	For processing exceptional events, which require that the device send a message back to the application. The application must explicitly ask for such events.

Table 5-2 (continued) DMediaPro Board Control Parameters/Value(s) and Use

Control Parameters	Range or Value(s)	Use
ML_QUEUE_SEND_COUNT_INT32	Number of messages in the queue.	Returns the number of items in the queue from the application to the device.
ML_QUEUE_RECEIVE_COUNT_INT32	Number of messages in the queue.	Returns the number of items (both replies and events) in the queue between the device and the application.
ML_QUEUE_SEND_WAITABLE_INT32	Number of messages in the queue.	Returns a ML waitable (a file descriptor in UNIX implementations). This occurs when more than N slots are free in the queue between the application and the device. This is used when an application needs to enqueue messages in chunks. The N setting is specified at open time via ML_OPEN_SEND_SIGNAL_COUNT.
ML_QUEUE_RECEIVE_WAITABLE_INT32	Number of messages in the queue.	Returns a ML waitable (a file descriptor in UNIX implementations). This occurs when an unread message from the device to the application is in the queue. Applications can wait on this, rather than polling for replies from the device.
ML_VIDEO_GENLOCK_TYPE_INT32	XTDIGVID_GENLOCK_SRC_TYPE_INTERNAL XTDIGVID_GENLOCK_SRC_TYPE_ANALOG XTDIGVID_GENLOCK_SRC_TYPE_DIGITAL_JACK_A XTDIGVID_GENLOCK_SRC_TYPE_DIGITAL_JACK_B	Sets the desired type of genlock sync source. Describes the genlock signal type. Only accepted on output paths. Each genlock type is specified as either a 32-bit resource ID or ML_VIDEO_GENLOCK_TYPE_INTERNAL.

Table 5-2 (continued) DMediaPro Board Control Parameters/Value(s) and Use

Control Parameters	Range or Value(s)	Use
ML_VIDEO_GENLOCK_SOURCE_TIMING_INT32	XTDIGVID_GENLOCK_TIMING_AUTODETECT ML_TIMING_525 ML_TIMING_625 ML_TIMING_1125_1920x1080_60i ML_TIMING_1125_1920x1080_5994i ML_TIMING_750_1280x720_60p ML_TIMING_750_1280x720_5994p ML_TIMING_1125_1920x1080_50i ML_TIMING_1125_1920x1080_25p ML_TIMING_1125_1920x1080_24p ML_TIMING_1125_1920x1080_2398p ML_TIMING_1125_1920x1035_5994i ML_TIMING_1125_1920x1080_24PsF ML_TIMING_1125_1920x1080_2398PsF ML_TIMING_1125_1920x1080_25PsF	Describes the genlock source timing. Only accepted on output paths. Each genlock source is specified as an output timing on the path and corresponds to the same timings that are provided for ML_VIDEO_TIMING_INT32.
ML_VIDEO_H_PHASE_I NT32	Defined by selected timing.	Sets or gets the video signal horizontal phase relative to the genlock offset.
ML_VIDEO_V_PHASE_I NT32	Defined by selected timing.	Sets or gets the video signal vertical phase relative to the genlock offset.

Table 5-2 (continued) DMediaPro Board Control Parameters/Value(s) and Use

Control Parameters	Range or Value(s)	Use
ML_VIDEO_OUTPUT_REPEAT_INT32	ML_VIDEO_REPEAT_NONE ML_VIDEO_REPEAT_FIELD ML_VIDEO_REPEAT_FRAME	<p>Controls whether the system repeats DMbuffers when the output is underflowing. If the application is performing output, and fails to provide buffers fast enough (the queue to the device under-flows), then this control determines the device behavior.</p> <p>ML_VIDEO_REPEAT_NONE The device does nothing, usually resulting in black output.</p> <p>ML_VIDEO_REPEAT_FIELD The device repeats the last field for interlaced non-interleaved transfers. For progressive signals or interleaved formats, this is the same as ML_VIDEO_REPEAT_FRAME.</p> <p>ML_VIDEO_REPEAT_FRAME The device repeats the last two fields This output capability is device dependent. The allowable settings should be queried via the get capabilities of ML_VIDEO_OUTPUT_REPEAT_INT32. On input, any signal outside the clipping region is simply ignored. On output, specific parameters control the generated signal. For more information on these parameters, see the <i>ML Programmer's Guide</i>.</p>
XTDIGVID_EE_MODE_INT32	XTDIGVID_EE_MODE_DISABLE XTDIGVID_EE_MODE_ENABLE	Loop-through serial input to serial output.
XTDIGVID_FF_MODE_INT32	XTDIGVID_FF_MODE_DISABLE XTDIGVID_FF_MODE_ENABLE	Field/Frame mode. Assists an application in performing 3/2 pulldown on output.

Table 5-2 (continued) DMediaPro Board Control Parameters/Value(s) and Use

Control Parameters	Range or Value(s)	Use
XTDIGVID_ LOOPBACK_INT32	XTDIGVID_LOOPBACK_DISABLE XTDIGVID_LOOPBACK_ENABLE	Sends the VBOB LVDS input (DMediaPro output) to the VBOB LVDS output.
ML_VIDEO_ GENLOCK_SIGNAL_ PRESENT_INT32	ML_TIMING_NONE ML_TIMING_UNKNOWN ML_TIMING_525 ML_TIMING_625 ML_TIMING_1125_1920x1080_60i ML_TIMING_1125_1920x1080_5994i ML_TIMING_750_1280x720_60p ML_TIMING_750_1280x720_5994p ML_TIMING_1125_1920x1080_50i ML_TIMING_1125_1920x1080_25p ML_TIMING_1125_1920x1080_24p ML_TIMING_1125_1920x1080_2398p ML_TIMING_1125_1920x1035_5994i ML_TIMING_1125_1920x1080_24PsF ML_TIMING_1125_1920x1080_2398PsF	These are read-only controls on the video output path. getControls returns the timing on the currently selected genlock jack. This control only functions after opening a path.

Table 5-2 (continued) DMediaPro Board Control Parameters/Value(s) and Use

Control Parameters	Range or Value(s)	Use
ML_VIDEO_SIGNAL_PRESENT_INT32	ML_TIMING_NONE ML_TIMING_UNKNOWN ML_TIMING_525 ML_TIMING_625 ML_TIMING_1125_1920x1080_60i ML_TIMING_1125_1920x1080_5994i ML_TIMING_750_1280x720_60p ML_TIMING_750_1280x720_5994p ML_TIMING_1125_1920x1080_50i ML_TIMING_1125_1920x1080_25p ML_TIMING_1125_1920x1080_24p ML_TIMING_1125_1920x1080_2398p ML_TIMING_1125_1920x1035_5994i ML_TIMING_1125_1920x1080_24PsF ML_TIMING_1125_1920x1080_2398PsF	These are read-only controls on the video input path. <code>getControls</code> returns the detected timing on the currently selected input jack. This control only functions after opening a path.
XTDIGVID_GENLOCK_STATE_INT32	XTDIGVID_GENLOCK_STATE_IS_UNLOCKED XTDIGVID_GENLOCK_STATE_IS_LOCKED XTDIGVID_GENLOCK_STATE_IS_UNKNOWN	These are read-only controls on the video output paths. <code>getControls</code> returns the current genlock state of an open path. If <code>GENLOCK_TYPE</code> is <code>INTERNAL</code> , this control returns <code>*_UNLOCKED</code> .
XTDIGVID_GENLOCK_ERROR_STATUS_INT32	XTDIGVID_GENLOCK_ERROR_STATUS_NONE XTDIGVID_GENLOCK_ERROR_STATUS_NO_SIGNAL XTDIGVID_GENLOCK_ERROR_STATUS_UNKNOWN_SIGNAL XTDIGVID_GENLOCK_ERROR_STATUS_ILLEGAL_COMBINATION XTDIGVID_GENLOCK_ERROR_STATUS_TIMING_MISMATCH	These are read-only controls on the video output paths. This control can be used to query for the cause of a <code>SYNC_LOST</code> event. It can also be used to query for the cause of a <code>GENLOCK_STATE_IS_UNLOCKED</code> return when the expected return is <code>GENLOCK_STATE_IS_LOCKED</code> .
ML_OPEN_MODE_INT32	ML_MODE_RWE	The application's intended use for the device. This specifies that the board can only be opened in the RWE mode.

Table 5-2 (continued) DMediaPro Board Control Parameters/Value(s) and Use

Control Parameters	Range or Value(s)	Use
ML_OPEN_SEND_QUEUE_COUNT_INT32	[2 - 1024]	This is the application's preferred size (number of messages) in the send queue. This affects the amount of memory allocated for this queue when the device is opened. The default is device-dependent.
ML_OPEN_RECEIVE_QUEUE_COUNT_INT32	[4 - 1024]	This is the application's preferred size (number of messages) in the receive queue. This affects the amount of memory allocated for this queue when the device is opened. The default is device-dependent. A null value indicates that the application does not expect to receive any events from a jack.
ML_OPEN_MESSAGE_PAYLOAD_SIZE_INT32	[1024 - 134217728]	This is the application's preferred size (in bytes) in the queue message payload area. This payload area holds messages in both the send and receive queues. The default is device-dependent.
ML_OPEN_EVENT_PAYLOAD_COUNT_INT32	[2 - 1024]	This is the application's preferred size (number of messages) in the queue event payload area. This payload area holds the contents of event messages in the receive queue. The default is device-dependent. A null value indicates that the application does not expect to receive any events from a jack.
ML_OPEN_SEND_SIGNAL_COUNT_INT32	[1 - 1024]	This is the application's preferred low-water level (number of empty message slots) in the send queue. When the device de-queues a message and causes the number of empty slots to exceed this level, then the device signals the send queue event. The default is device-dependent.

DMediaPro Default Path Controls

Following are the default values for the HD and SD input path controls.

HD Default Input Path Controls

```

ML_VIDEO_TIMING_INT32 = ML_TIMING_1125_1920x1080_5994i
ML_VIDEO_PRECISION_INT32 = 8
ML_VIDEO_COLORSPACE_INT32 = ML_COLORSPACE_CbYCr_709_HEAD
ML_IMAGE_TEMPORAL_SAMPLING_INT32 = ML_TEMPORAL_SAMPLING_FIELD_BASED
ML_VIDEO_SAMPLING_INT32 = ML_SAMPLING_422
ML_VIDEO_START_Y_F1_INT32 = 21
ML_VIDEO_START_Y_F2_INT32 = 584
ML_VIDEO_HEIGHT_F1_INT32 = 540
ML_VIDEO_HEIGHT_F2_INT32 = 540
ML_VIDEO_WIDTH_INT32 = 1920
ML_IMAGE_WIDTH_INT32 = 1920
ML_IMAGE_HEIGHT_1_INT32 = 1080
ML_IMAGE_HEIGHT_2_INT32 = 0
ML_IMAGE_PACKING_INT32 = ML_PACKING_8
ML_IMAGE_SAMPLING_INT32 = ML_SAMPLING_444
ML_IMAGE_COLORSPACE_INT32 = ML_COLORSPACE_RGB_709_FULL
ML_IMAGE_INTERLEAVE_MODE_INT32 = ML_INTERLEAVE_MODE_INTERLEAVED
ML_IMAGE_DOMINANCE_INT32 = ML_DOMINANCE_F1
ML_IMAGE_ORIENTATION_INT32 = ML_ORIENTATION_TOP_TO_BOTTOM
XTDIGVID_LOOPBACK_INT32 = XTDIGVID_LOOPBACK_DISABLE
ML_IMAGE_COMPRESSION_INT32 = ML_COMPRESSION_UNCOMPRESSED
ML_IMAGE_SKIP_PIXELS_INT32 = 0
ML_IMAGE_ROW_BYTES_INT32 = 0
ML_IMAGE_SKIP_ROWS_INT32 = 0
ML_VIDEO_START_X_INT32 = 1

```

SD Default Input Path Controls

```

ML_VIDEO_TIMING_INT32 = ML_TIMING_525
ML_VIDEO_PRECISION_INT32 = 8
ML_VIDEO_COLORSPACE_INT32 = ML_COLORSPACE_CbYCr_601_HEAD
ML_IMAGE_TEMPORAL_SAMPLING_INT32 = ML_TEMPORAL_SAMPLING_FIELD_BASED
ML_VIDEO_SAMPLING_INT32 = ML_SAMPLING_422
ML_VIDEO_START_Y_F1_INT32 = 20
ML_VIDEO_START_Y_F2_INT32 = 283
ML_VIDEO_HEIGHT_F1_INT32 = 244
ML_VIDEO_HEIGHT_F2_INT32 = 243

```

```
ML_VIDEO_WIDTH_INT32 = 720
ML_IMAGE_WIDTH_INT32 = 720
ML_IMAGE_HEIGHT_1_INT32 = 487
ML_IMAGE_HEIGHT_2_INT32 = 0
ML_IMAGE_PACKING_INT32 = ML_PACKING_8
ML_IMAGE_SAMPLING_INT32 = ML_SAMPLING_444
ML_IMAGE_COLORSPACE_INT32 = ML_COLORSPACE_RGB_601_FULL
ML_IMAGE_INTERLEAVE_MODE_INT32 = ML_INTERLEAVE_MODE_INTERLEAVED
ML_IMAGE_DOMINANCE_INT32 = ML_DOMINANCE_F1
ML_IMAGE_ORIENTATION_INT32 = ML_ORIENTATION_TOP_TO_BOTTOM
XTDIGVID_LOOPBACK_INT32 = XTDIGVID_LOOPBACK_DISABLE
ML_IMAGE_COMPRESSION_INT32 = ML_COMPRESSION_UNCOMPRESSED
ML_IMAGE_SKIP_PIXELS_INT32 = 0
ML_IMAGE_ROW_BYTES_INT32 = 0
ML_IMAGE_SKIP_ROWS_INT32 = 0
ML_VIDEO_START_X_INT32 = 1
```

Following are the default values for the HD and SD output path controls.

HD Default Output Path Controls

```
ML_VIDEO_TIMING_INT32 = ML_TIMING_1125_1920x1080_5994i
ML_VIDEO_PRECISION_INT32 = 8
ML_VIDEO_COLORSPACE_INT32 = ML_COLORSPACE_CbYCr_709_HEAD
ML_IMAGE_TEMPORAL_SAMPLING_INT32 = ML_TEMPORAL_SAMPLING_FIELD_BASED
ML_VIDEO_SAMPLING_INT32 = ML_SAMPLING_422
ML_VIDEO_START_Y_F1_INT32 = 21
ML_VIDEO_START_Y_F2_INT32 = 584
ML_VIDEO_HEIGHT_F1_INT32 = 540
ML_VIDEO_HEIGHT_F2_INT32 = 540
ML_VIDEO_WIDTH_INT32 = 1920
ML_IMAGE_WIDTH_INT32 = 1920
ML_IMAGE_HEIGHT_1_INT32 = 1080
ML_IMAGE_HEIGHT_2_INT32 = 0
ML_IMAGE_PACKING_INT32 = ML_PACKING_8
ML_IMAGE_SAMPLING_INT32 = ML_SAMPLING_444
ML_IMAGE_COLORSPACE_INT32 = ML_COLORSPACE_RGB_709_FULL
ML_IMAGE_INTERLEAVE_MODE_INT32 = ML_INTERLEAVE_MODE_INTERLEAVED
ML_IMAGE_DOMINANCE_INT32 = ML_DOMINANCE_F1
ML_IMAGE_ORIENTATION_INT32 = ML_ORIENTATION_TOP_TO_BOTTOM
ML_VIDEO_GENLOCK_TYPE_INT32 = XTDIGVID_GENLOCK_SRC_TYPE_INTERNAL
ML_VIDEO_GENLOCK_SOURCE_TIMING_INT32 = ML_TIMING_1125_1920x1080_5994i
ML_VIDEO_OUTPUT_REPEAT_INT32 = ML_VIDEO_REPEAT_NONE
XTDIGVID_EE_MODE_INT32 = XTDIGVID_EE_MODE_DISABLE
```

```

XTDIGVID_FF_MODE_INT32 = XTDIGVID_FF_MODE_DISABLE
ML_IMAGE_COMPRESSION_INT32 = ML_COMPRESSION_UNCOMPRESSED
ML_IMAGE_SKIP_PIXELS_INT32 = 0
ML_IMAGE_ROW_BYTES_INT32 = 0
ML_IMAGE_SKIP_ROWS_INT32 = 0
ML_VIDEO_START_X_INT32 = 1

```

SD Default Output Path Controls

```

ML_VIDEO_TIMING_INT32 = ML_TIMING_525
ML_VIDEO_PRECISION_INT32 = 8
ML_VIDEO_COLORSPACE_INT32 = ML_COLORSPACE_CbYCr_601_HEAD
ML_IMAGE_TEMPORAL_SAMPLING_INT32 = ML_TEMPORAL_SAMPLING_FIELD_BASED
ML_VIDEO_SAMPLING_INT32 = ML_SAMPLING_422
ML_VIDEO_START_Y_F1_INT32 = 20
ML_VIDEO_START_Y_F2_INT32 = 283
ML_VIDEO_HEIGHT_F1_INT32 = 244
ML_VIDEO_HEIGHT_F2_INT32 = 243
ML_VIDEO_WIDTH_INT32 = 720
ML_IMAGE_WIDTH_INT32 = 720
ML_IMAGE_HEIGHT_1_INT32 = 487
ML_IMAGE_HEIGHT_2_INT32 = 0
ML_IMAGE_PACKING_INT32 = ML_PACKING_8
ML_IMAGE_SAMPLING_INT32 = ML_SAMPLING_444
ML_IMAGE_COLORSPACE_INT32 = ML_COLORSPACE_RGB_601_FULL
ML_IMAGE_INTERLEAVE_MODE_INT32 = ML_INTERLEAVE_MODE_INTERLEAVED
ML_IMAGE_DOMINANCE_INT32 = ML_DOMINANCE_F1
ML_IMAGE_ORIENTATION_INT32 = ML_ORIENTATION_TOP_TO_BOTTOM
ML_VIDEO_GENLOCK_TYPE_INT32 = XTDIGVID_GENLOCK_SRC_TYPE_INTERNAL
ML_VIDEO_GENLOCK_SOURCE_TIMING_INT32 = ML_TIMING_525
ML_VIDEO_OUTPUT_REPEAT_INT32 = ML_VIDEO_REPEAT_NONE
XTDIGVID_EE_MODE_INT32 = XTDIGVID_EE_MODE_DISABLE
XTDIGVID_FF_MODE_INT32 = XTDIGVID_FF_MODE_DISABLE
ML_IMAGE_COMPRESSION_INT32 = ML_COMPRESSION_UNCOMPRESSED
ML_IMAGE_SKIP_PIXELS_INT32 = 0
ML_IMAGE_ROW_BYTES_INT32 = 0
ML_IMAGE_SKIP_ROWS_INT32 = 0
ML_VIDEO_START_X_INT32 = 1

```

ML_TIMING

The ML_TIMING control sets the timing type, which expresses the timing of video presented to an input or an output.

Each value for ML_TIMING indicates the raster configuration of a particular SMPTE specification, such as SMPTE 274M-1995. The values are named according to the raster format:

- The first field is the number of total lines, such as 1125, 750, 525, or 625.
- The second field is the size of the active region, in pixels by lines.
- The third field is the vertical refresh rate and the scanning format; the scanning format is as follows:
 - i: interlaced
 - p: progressive (noninterlaced)
 - PsF: Progressive segmented Frame

In Progressive segmented Frame (PsF) formats, the frame is transmitted as two fields that are of the same time instant, while in interlaced formats the two fields are temporally displaced.

For example, ML_TIMING_1125_1920x1080_5994i specifies 1125 total lines, an active region of 1920 pixels by 1080 lines, 59.94 fields per second, and 2:1 interlacing.

Note: If you change the ML_TIMING from SD to HD or HD to SD at the beginning of a data transfer, several seconds may elapse before the change takes effect.

Input Timing Auto Detect

The DMediaPro Board Input Timing Auto Detect function checks whether the detected signal matches the user requested signal. If the detected signal does not match the requested signal, there are two possible results:

- If the application is registered for SYNC_LOST events on the input path, the application receives a SYNC_LOST event.
- If the device is not looking for a SYNC_LOST event, a ML_DEVICE error is sent to the application. If an error is detected before a transfer is started, the dmmodule does not allow the transfer to begin.

For more information on input timing-related events and device errors, see “DMediaPro Events” on page 81.

Genlock

Genlock enables the SGI VBOB to receive an external sync signal, which locks the timing of the output video picture. This allows you to maintain a common timing across multiple video devices. With the DMediaPro/VBOB system, you can set up genlock as follows:

- SD output
 - ML_TIMING_525 locked to an NTSC reference connected to the VBOB SD video input or SD genlock input
 - ML_TIMING_625 locked to a PAL reference connected to the VBOB SD video input or SD genlock input
- HD output
 - Supported genlock input timings (see Table 5-3) referenced by the VBOB HD video input or HD genlock input and locked to a compatible video output timing. The only exceptions are ML_TIMING_525 and ML_TIMING_625, which can be used only as a reference on the VBOB HD genlock input, but not on the VBOB HD video input.

Table 5-3 lists each of the supported genlock input timings and their compatible HD video output timings. The prefix, ML_TIMING_ should appear before each timing, but was omitted to avoid redundancy.

Table 5-3 Supported HD Input/Output Timings

Genlock Input Timing	Video Output Timing
525	1125_1920x1080_5994i 750_1280x720_5994p 1125_1920x1080_2398p 1125_1920x1080_2398PsF 1125_1920x1035_5994i
625	1125_1920x1080_50i 1125_1920x1080_25p 1125_1920x1080_25PsF
750_1280x720_60p	750_1280x720_60p 1125_1920x1080_24p 1125_1920x1080_24PsF 1125_1920x1080_60i
750_1280x720_5994p	750_1280x720_5994p 1125_1920x1035_5994i 1125_1920x1080_5994i 1125_1920x1080_2398p 1125_1920x1080_2398PsF
1125_1920x1080_5994i	750_1280x720_5994p 1125_1920x1035_5994i 1125_1920x1080_5994i 1125_1920x1080_2398p 1125_1920x1080_2398PsF
1125_1920x1080_2398p	1125_1920x1080_2398p 1125_1920x1080_2398PsF
1125_1920x1080_2398PsF	1125_1920x1080_2398PsF 1125_1920x1080_2398p
1125_1920x1080_24p	1125_1920x1080_24p 1125_1920x1080_24PsF

Table 5-3 (continued) Supported HD Input/Output Timings

Genlock Input Timing	Video Output Timing
1125_1920x1080_24PsF	1125_1920x1080_24PsF 1125_1920x1080_24p
1125_1920x1080_50i	1125_1920x1080_50i 1125_1920x1080_25p 1125_1920x1080_25PsF
1125_1920x1080_60i	1125_1920x1080_60i 750_1280x720_60p 1125_1920x1080_24p 1125_1920x1080_24PsF
1125_1920x1035_5994i	1125_1920x1035_5994i 750_1280x720_5994p 1125_1920x1080_2398p 1125_1920x1080_2398PsF 1125_1920x1080_5994i
1125_1920x1080_25p	1125_1920x1080_25p 1125_1920x1080_25PsF 1125_1920x1080_50i
1125_1920x1080_25 PsF	1125_1920x1080_25p 1125_1920x1080_25PsF 1125_1920x1080_50i

Genlock Auto Detect

The DMediaPro Board Genlock Auto Detect function automatically identifies the genlock input signal, (genlock source timing) and determines whether the signal is compatible with the video output signal. If the DMediaPro Board determines that the two signals are compatible, the board automatically locks the genlock source timing with the video output timing.

To enable this function, set the `ML_VIDEO_GENLOCK_SOURCE_TIMING_INT32` control parameter to the `XTDIGVID_GENLOCK_TIMING_AUTODETECT` value (see Table 5-2).

For more information on genlock-related events and device errors, see “DMediaPro Events” on page 81.

ML_IMAGE_PACKING

In ML, the combination of `ML_IMAGE_PACKING`, and `ML_IMAGE_SAMPLING` is the equivalent to `VL_PACKING` in the VL environment. Table 5-4 shows how the ML combinations correspond to VL packing. If you are unfamiliar with `VL_PACKING`, see the *HD I/O Board Owner’s Guide* for a detailed description.

Table 5-4 VL/ML Packing Conversions

<code>VL_PACKING</code>	<code>ML_IMAGE_PACKING</code>	<code>ML_IMAGE_SAMPLING</code>
<code>VL_PACKING_R242_8</code>	<code>ML_PACKING_8</code>	<code>ML_SAMPLING_422</code>
<code>VL_PACKING_242_8</code>	<code>ML_PACKING_8_3214</code>	<code>ML_SAMPLING_422</code>
<code>VL_PACKING_R242_10</code>	<code>ML_PACKING_10</code>	<code>ML_SAMPLING_422</code>
<code>VL_PACKING_242_10</code>	<code>ML_PACKING_10_3214</code>	<code>ML_SAMPLING_422</code>
<code>VL_PACKING_R242_10_in_16_L</code>	<code>ML_PACKING_10in16L</code>	<code>ML_SAMPLING_422</code>
<code>VL_PACKING_242_10_in_16_L</code>	<code>ML_PACKING_10in16L_3214</code>	<code>ML_SAMPLING_422</code>
<code>VL_PACKING_R242_10_in_16_R</code>	<code>ML_PACKING_10in16R</code>	<code>ML_SAMPLING_422</code>
<code>VL_PACKING_242_10_in_16_R</code>	<code>ML_PACKING_10in16R_3214</code>	<code>ML_SAMPLING_422</code>
<code>VL_PACKING_R2424_10_10_10_2Z</code>	<code>ML_PACKING_10_10_10_2</code>	<code>ML_SAMPLING_4224</code>

Table 5-4 (continued) VL/ML Packing Conversions

VL_PACKING	ML_IMAGE_PACKING	ML_IMAGE_SAMPLING
VL_PACKING_2424_10_10_10_2Z	ML_PACKING_10_10_10_2_3214	ML_SAMPLING_4224
VL_PACKING_444_8	ML_PACKING_8	ML_SAMPLING_444
VL_PACKING_R444_8	ML_PACKING_8_R	ML_SAMPLING_444
VL_PACKING_444_12_in_16L	ML_PACKING_S12in16L	ML_SAMPLING_444
VL_PACKING_444_12_in_16_R	ML_PACKING_S12in16R	ML_SAMPLING_444
VL_PACKING_4444_8	ML_PACKING_8	ML_SAMPLING_4444
VL_PACKING_R4444_8	ML_PACKING_8_R	ML_SAMPLING_4444
VL_PACKING_4444_10_10_10_2	ML_PACKING_10_10_10_2	ML_SAMPLING_4444
VL_PACKING_R4444_10_10_10_2	ML_PACKING_10_10_10_2_R	ML_SAMPLING_4444

Note: If you change packings at the beginning of a data transfer, several seconds may elapse before the change takes effect.

ML_COLORSPACE

The ML_COLORSPACE control specifies the color space of video data in memory or for input and output. A color space is a color component encoding format, for example, RGB and YUV. Because video equipment uses more than one color space, the DMediaPro video paths, in addition to the image memory buffers, support the ML_COLORSPACE control.

Each component of an image has:

- A color that it represents
- A canonical minimum value
- A canonical maximum value

Normally, a component stays within the minimum and maximum values. For example, for a luma signal such as Y, you can think of these limits as the black level and the peak white level, respectively. For an unsigned component with n bits, you can determine the full range minimum value, maximum value as follows:

$[0, (2^n)-1]$

This provides the maximum resolution for each component.

Color Spaces and Color Models

Various HDTV specifications define color models differently from those defined in Recommendation 601 (ITU-R BT.601-5), which is used by most Standard Definition digital video equipment. For HDTV, the DMediaPro Board supports the following three color models:

- SMPTE 240M
- Recommendation 709 (ITU-R BT.709-2)
- Recommendation 601 (ITU-R BT.601-5)

Within each color model, four different color spaces exist:

- YCrCb: headroom range
Headroom range means that black is at, for example, code 64 rather than 0, and white is at, for example, code 940 rather than 1023. Headroom-range color spaces can accommodate overshoot (superwhite) and undershoot (superblack) colors. Full-range color spaces clamp these out-of-range colors to black and white.
- YUV: full range
- RGB_H: headroom range
- RGB_F: full range

For image memory buffers, these four color spaces are defined for each of three color models, resulting in 12 color spaces. Note that all 12 are supported on image memory buffers, but only YCrCb and RGB_H color spaces are supported on video paths.

Color space conversion is performed within a color model if the color spaces are different on the image memory buffer and video paths. Conversion between the color models is not supported.

Note: If you change this control at the beginning of a data transfer, several seconds may elapse before the change takes effect.

Typically, two sets of colors are used together, RGB (RGBA) and YCrCb/YUV (VYUA). YCrCb (YUV), the most common representation of color from the video world, represents each color by a luma component called Y and two components of chroma, called Cr (or V), and Cb (or U). The luma component is loosely related to brightness or luminance, and the chroma components make up a quantity loosely related to hue. These components are defined in ITU-R BT.601-5 (also known as Rec. 601 and CCIR 601), ITU-R BT.709-2, and SMPTE 240M.

The alpha channel is not a real color. For that channel, the minimum value specifies completely transparent, and the maximum value specifies completely opaque.

For more information about color spaces, see *A Technical Introduction to Digital Video*, by Charles A. Poynton (New York: Wiley, 1996).

ML_COLORSPACE Control of Blanking

Along with image memory buffer color space, ML_COLORSPACE determines the color-conversion matrix values. In addition, this control affects the type of blanking output by the board during horizontal and vertical blanking, and during active video area when not transferring data. On a video output path, ML_COLORSPACE affects the type of blanking that the board outputs, in accordance with SMPTE 274M:

- YCrCb: blanking is $Y = 64$, $Cr/Cb = 512$, $A = 64$
- RGB_H: blanking is $R = 64$, $G = 64$, $B = 64$, $A = 64$

ML_COLORSPACE and Lookup Tables

The DMediaPro Board supports Lookup Tables (LUTs) on input and output for gamma correction or decorection. To successfully run an application with linear components, you can use LUTs to convert between linear and nonlinear spaces.

The DMediaPro hardware includes a separate LUT for each RGB color component. Each of the three LUTs is a table of 8,192 entries; each entry stores 13 bits. The application programs the entries in each table. The LUTs produce offsets, if they are required by the memory storage format.

The LUTs perform rounding as follows:

- If the LUT is not explicitly programmed by the application, the output LUT is in pass-through mode, all rounding is performed in the color space converter, and the input LUT performs both rounding and offset.
- If the LUT is programmed explicitly by the application, the application can control rounding as part of the Lookup Table Function. The packer (hardware that reads the LUT and formats data for the host memory; see Figure 5-3) performs a final conversion from 13-bit LUT format to host memory format.

An application can also use the LUT to convert between video path RGB_H and image memory buffer RGB_F. Because each component is independent of the others for this conversion, a matrix multiplication is not needed (pass-through mode). The required component scaling and rounding can be placed into each LUT.

ML_COLORSPACE Example

Figure 5-3 shows an example color space conversion. In the example, RGB are values in linear space and R'G'B' are values in nonlinear space after the opto-electric transfer function is applied as specified in ITU-R BT.709. You can use the LUTs to apply this function or its inverse to convert between RGB and R'G'B'.

This example also shows a typical video capture path. The input jack is YCrCb 4:2:2 and the desired result in system memory is RGB. First, an appropriate filter interpolates YCrCb 4:2:2 to YCrCb 4:4:4 to fill in the missing CrCb samples. Then a 3x3 matrix multiplier with appropriate offsets and coefficients obtains RGB values for each pixel. At this point, you can use the LUT option to convert gamma pre-corrected RGB values to linear RGB values. Finally, the packer swizzles the bits into the desired memory packing format and DMA places the result in system memory.



Figure 5-3 Color Space Conversion Example

Field Dominance

Field dominance identifies the frame boundaries in a field sequence; that is, it specifies which pair of fields in a field sequence constitutes a frame. You can use `ML_IMAGE_DOMINANCE_INT32` to specify where an edit occurs, as follows:

- `ML_DOMINANCE_F1`: The edit occurs on the nominal video field boundary (field 1, or F1).
- `ML_DOMINANCE_F2`: The edit occurs on the intervening field boundary (field 2, or F2).

You can determine whether a field is field 1 or field 2 by setting bit 9, the F bit, in the XYZ word of the EAV and SAV sequences, as follows:

- For field 1 (also called the odd field), set the F bit to 0.
- For field 2 (also called the even field), set the F bit to 1.

Note: Field dominance has no effect on progressive timings.

Figure 5-4 shows fields and frames as defined for digital 1080-line formats for the DMediaPro Board.

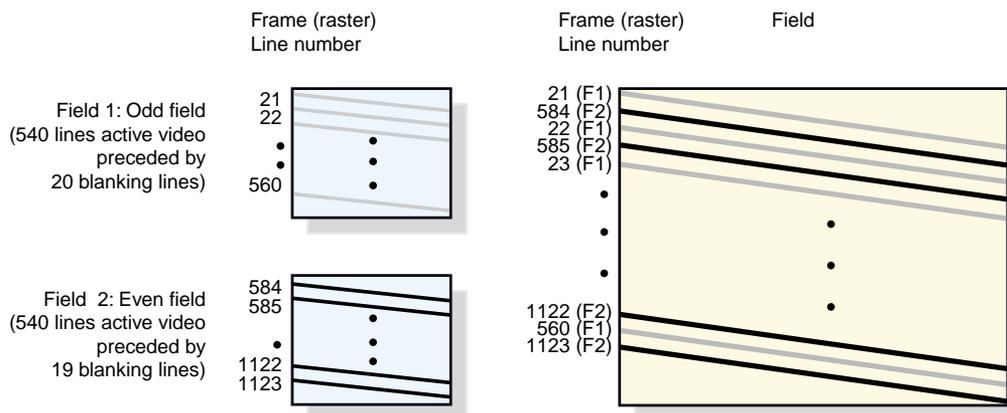


Figure 5-4 Fields and Frames for SMPTE 274M

Editing is usually on field 1 boundaries, where field 1 is defined as the first field in the video standard's two-field output sequence. However, you may want to edit on F2 boundaries, which fall on the field between the video standard's frame boundary. To do so, use this control, then program your deck to select F2 edits.

A set of frames for output must be de-interlaced into fields differently, depending on the specified output field dominance. For SMPTE 274M, the top line is in F1, as shown in Figure 5-4. For SMPTE 240M, the top line is in F2. For example, when F1 dominance is selected, the field with the topmost line must be the first field to be transferred; when F2 dominance is selected, the field with the topmost line must be the second field to be transferred.

EE Mode

The DMediaPro Board supports an EE mode (XTDIGVID_EE_MODE_INT32). In this mode, the serial input is looped-through directly to the serial output. EE mode can only function correctly if the LVDS output is genlocked to the same source as the device feeding the LVDS input. This genlock mode is commonly referred to as "reclocking," which is used in DAs, D to As, and data serializers. Reclocking ensures that the re-transmitted signals have sufficient jitter attenuation applied to reject jitter from the digital inputs.

When using EE mode, you must consider the following issues.

- The dmmodule does not enforce the genlock requirement. You can enable EE mode, but the output display may be unstable.
- You can enable EE mode while an output transfer is running. For example, if an SD output transfer is running and SD EE mode is enabled on the output path, EE mode "hijacks" the serial output jack.

Automatically Correcting for Output Underflow

If the application is not sending buffers fast enough for the receiving equipment's video frame rate, you can set `ML_VIDEO_OUTPUT_REPEAT_INT32` to repeat MLbuffers automatically. The values for this control vary, depending on whether the transfer is progressive or interlaced.

- `ML_VIDEO_REPEAT_NONE`
Repeats nothing, usually resulting in black output. This is the most useful for debugging, because underflow is then quite visible on output
- `ML_VIDEO_REPEAT_FIELD`
Repeats the last field (non-interleaved) or the last frame (interleaved or progressive). This setting is spacially imperfect, but does not cause flicker.
- `ML_REPEAT_FRAME` (the default)
Repeats the last two fields (non-interleaved) or the last frame (interleaved or progressive). This setting is spacially better than `ML_VIDEO_REPEAT_FIELD`, but causes flicker.

Capturing Graphics to Video

To capture graphics to video, you can use OpenGL to read pixels into memory. However, the coordinate system differs between video and Open GL; under OpenGL, the origin is at the lower left corner and, in video, the origin is in the upper left corner. To adjust for this difference, set the `ML_IMAGE_ORIENTATION_INT32` parameter to `ML_BOTTOM_TO_TOP`. For more information, see Table 5-2 in this guide and the *ML Programmer's Guide*.

Note: If you have an HD GVO Board (DG5-2/TVO) with an SGI Video Breakout Box installed in an SGI Onyx compatible system, it is easier to capture graphics to video using the HD GVO system. For more information, see the *SGI HD GVO Owner's Guide*.

DMediaPro Events

In some cases, an exceptional event occurs, which requires the device to send a message back to the application. For this type of event message, you must initiate a request. When the application requests an event, it must read its receive queue often enough to prevent the device from running out of the required message space for the specific enqueue request. If the queue begins to fill up, the device enqueues an event message, which terminates the exceptional event.

The device does not have to allocate space in the data area for reply messages. It automatically stops sending notifications of events when the receive queue begins to fill up. Space is reserved in the receive queue for a reply to every message that the application enqueues. When there is insufficient space, any attempt to send new messages fails.

The DMediaPro Board currently supports the following ML exceptional events:

```
ML_EVENT_VIDEO_SEQUENCE_LOST
ML_EVENT_VIDEO_SYNC_LOST
ML_EVENT_VIDEO_SYNC_GAINED
```

Table 5-5 summarizes these events.

Table 5-5 DMediaPro Events

Event	Use
ML_EVENT_VIDEO_SEQUENCE_LOST	A field/frame was dropped.
ML_EVENT_VIDEO_SYNC_LOST	Genlock was lost or the input signal was lost.
ML_EVENT_VIDEO_SYNC_GAINED	Genlock sync lock occurred or a valid signal was found on the input.

Note: Other events, for example, `ML_BUFFERS_COMPLETE`, are automatically sent to the application. For more information, see the *ML Programmer's Guide*.

Following are the ML controls and event records:

```
event == ML_EVENT_VIDEO_SEQUENCE_LOST
```

```
    eventRecord[0].param = ML_VIDEO_UST_INT64;  
    eventRecord[0].value.int64 = ust;  
    eventRecord[0].length = 1;  
    eventRecord[1].param = ML_VIDEO_MSC_INT64;  
    eventRecord[1].value.int64 = msc;  
    eventRecord[1].length = 1;  
    eventRecord[2].param = ML_END;
```

```
event == ML_EVENT_VIDEO_SYNC_GAINED, ML_EVENT_VIDEO_SYNC_LOST (output  
path)
```

```
    eventRecord[0].param = ML_VIDEO_GENLOCK_SIGNAL_PRESENT_INT32;  
    eventRecord[0].value.int32 = <detectedTiming> (see Table 5-2)  
    eventRecord[0].length = 1;  
    eventRecord[1].param = XTDIGVID_GENLOCK_ERROR_STATUS_INT32;  
    eventRecord[1].value.int32 = <syncLostReason> (see Table 5-6)  
    eventRecord[1].length = 1;  
    eventRecord[2].param = ML_END;
```

```
event == ML_EVENT_VIDEO_SYNC_GAINED, ML_EVENT_VIDEO_SYNC_LOST (input  
path)
```

```
    eventRecord[0].param = ML_VIDEO_SIGNAL_PRESENT_INT32;  
    eventRecord[0].value.int32 = <detectedTiming> (see Table 5-2)  
    eventRecord[0].length = 1;  
    eventRecord[1].param = ML_END;
```

Table 5-6 describes the XTDIGVID_GENLOCK_ERROR_STATUS_INT32 values for ML_EVENT_VIDEO_SYNC_LOST on the output path. It also shows the corresponding values for ML_VIDEO_GENLOCK_SIGNAL_PRESENT_INT32.

Table 5-6 Error Status Values for ML_EVENT_VIDEO_SYNC_LOST (output path)

Error Status Values	ML_VIDEO_GENLOCK_SIGNAL_PRESENT_INT32
XTDIGVID_GENLOCK_ERROR_STATUS_NO_SIGNAL (No signal detected on specified genlock jack)	ML_TIMING_NONE
XTDIGVID_GENLOCK_ERROR_STATUS_UNKNOWN_SIGNAL (Unknown signal detected or unable to identify the signal on a specified genlock jack)	ML_TIMING_UNKNOWN
XTDIGVID_GENLOCK_ERROR_STATUS_ILLEGAL_COMBINATION (Detected signal on the genlock jack is an illegal or unsupported combination for the specified output timing)	ID of the timing detected on the genlock jack
XTDIGVID_GENLOCK_ERROR_STATUS_TIMING_MISMATCH (Detected signal does not match the user's request using the ML_VIDEO_GENLOCK_SOURCE_TIMING_INT32 parameter)	ID of the timing detected on the genlock jack
XTDIGVID_GENLOCK_ERROR_STATUS_NONE (No Error Status)	ID of the timing detected on the genlock jack

Examples

This section provides the following examples:

- “Capturing 487 Line 525” on page 84
- “Playback from Memory to Video” on page 85
- “Re-sizing Field Height” on page 86
- “Programmable Lookup Tables (LUTs)” on page 88
- “FF Mode” on page 89
- “Setting Controls on a Jack” on page 90

Capturing 487 Line 525

Following are the ML control settings for capturing 487 line 525:

```
ML_VIDEO_TIMING_INT32 = ML_TIMING_525
ML_VIDEO_COLORSPACE_INT32 = ML_COLORSPACE_CbYCr_601_HEAD
ML_VIDEO_PRECISION_INT32 = 8
ML_VIDEO_START_Y_F1_INT32 = 20
ML_VIDEO_START_Y_F2_INT32 = 283
ML_VIDEO_HEIGHT_F1_INT32 = 244
ML_VIDEO_HEIGHT_F2_INT32 = 243
ML_IMAGE_TEMPORAL_SAMPLING_INT32 = ML_TEMPORAL_SAMPLING_FIELD_BASED
ML_VIDEO_SAMPLING_INT32 = ML_SAMPLING_422
ML_VIDEO_WIDTH_INT32 = 720
ML_IMAGE_WIDTH_INT32 = 720
ML_IMAGE_HEIGHT_1_INT32 = 487
ML_IMAGE_HEIGHT_2_INT32 = 0
ML_IMAGE_SAMPLING_INT32 = ML_SAMPLING_444
ML_IMAGE_COLORSPACE_INT32 = ML_COLORSPACE_RGB_601_FULL
ML_IMAGE_PACKING_INT32 = ML_PACKING_8
ML_IMAGE_INTERLEAVE_MODE_INT32 = ML_INTERLEAVE_MODE_INTERLEAVED
ML_IMAGE_DOMINANCE_INT32 = ML_DOMINANCE_F1
ML_IMAGE_ORIENTATION_INT32 = ML_ORIENTATION_TOP_TO_BOTTOM
XTDIGVID_LOOPBACK_INT32 = XTDIGVID_LOOPBACK_DISABLE
ML_IMAGE_COMPRESSION_INT32 = ML_COMPRESSION_UNCOMPRESSED
ML_IMAGE_ROW_BYTES_INT32 = 0
ML_IMAGE_SKIP_PIXELS_INT32 = 0
ML_IMAGE_SKIP_ROWS_INT32 = 0
ML_VIDEO_START_X_INT32 = 1
```

Playback from Memory to Video

Following are the ML control settings for performing a memory to video transfer in HD 720p format:

```
ML_VIDEO_TIMING_INT32 = ML_TIMING_750_1280x720_5994p
ML_VIDEO_PRECISION_INT32 = 8
ML_VIDEO_COLORSPACE_INT32 = ML_COLORSPACE_CbYCr_709_HEAD
ML_IMAGE_TEMPORAL_SAMPLING_INT32 = ML_TEMPORAL_SAMPLING_PROGRESSIVE
ML_VIDEO_SAMPLING_INT32 = ML_SAMPLING_422
ML_VIDEO_START_Y_F1_INT32 = 26
ML_VIDEO_START_Y_F2_INT32 = 0
ML_VIDEO_HEIGHT_F1_INT32 = 720
ML_VIDEO_HEIGHT_F2_INT32 = 0
ML_VIDEO_WIDTH_INT32 = 1280
ML_IMAGE_WIDTH_INT32 = 1280
ML_IMAGE_HEIGHT_1_INT32 = 720
ML_IMAGE_HEIGHT_2_INT32 = 0
ML_IMAGE_PACKING_INT32 = ML_PACKING_8
ML_IMAGE_SAMPLING_INT32 = ML_SAMPLING_444
ML_IMAGE_COLORSPACE_INT32 = ML_COLORSPACE_RGB_709_FULL
ML_IMAGE_INTERLEAVE_MODE_INT32 = ML_INTERLEAVE_MODE_INTERLEAVED
ML_IMAGE_DOMINANCE_INT32 = ML_DOMINANCE_F1
ML_IMAGE_ORIENTATION_INT32 = ML_ORIENTATION_TOP_TO_BOTTOM
ML_VIDEO_GENLOCK_TYPE_INT32 = XTDIGVID_GENLOCK_SRC_TYPE_INTERNAL
ML_VIDEO_GENLOCK_SOURCE_TIMING_INT32 = ML_TIMING_525
XTDIGVID_FF_MODE_INT32 = XTDIGVID_FF_MODE_DISABLE
ML_VIDEO_OUTPUT_REPEAT_INT32 = ML_VIDEO_REPEAT_NONE
ML_IMAGE_COMPRESSION_INT32 = ML_COMPRESSION_UNCOMPRESSED
ML_IMAGE_ROW_BYTES_INT32 = 0
ML_IMAGE_SKIP_PIXELS_INT32 = 0
ML_IMAGE_SKIP_ROWS_INT32 = 0
ML_VIDEO_START_X_INT32 = 1
```

Re-sizing Field Height

The DMediaPro Board uses the standard NTSC field height of 487 lines for Standard Definition video. However, some SGI products (for example, DIVO and DIVO DVC), use a 486 line NTSC field height. The following example provides ML code that you can use to retrieve the default sizing parameters for any given timing. Then you can reset these parameters from 487 lines to 486 lines, which provides backward compatibility with SGI Standard Definition products, such as DIVO and DIVO DVC.

Note: This example is the accepted method for retrieving these values, so you do not have to perform any calculations.

```
// timing = ML_TIMING_525

short progressive;

Dmpv videoSizeDefaults[] = {
    ML_IMAGE_TEMPORAL_SAMPLING_INT32, 0, 0, 0,
    ML_VIDEO_START_Y_F1_INT32, 0, 0, 0,
    ML_VIDEO_START_Y_F2_INT32, 0, 0, 0,
    ML_VIDEO_HEIGHT_F1_INT32, 0, 0, 0,
    ML_VIDEO_HEIGHT_F2_INT32, 0, 0, 0,
    ML_VIDEO_WIDTH_INT32, 0, 0, 0,
    ML_END, 0, 0, 0
};

if (starty1 != NULL) {
    *tempSampling = videoSizeDefaults[0].value.int32;
    progressive = (*tempSampling == ML_TEMPORAL_SAMPLING_PROGRESSIVE);
    *starty1 = videoSizeDefaults[1].value.int32;
    /* set starty2 to 0 if progressive, func returns -1 */
    *starty2 = (progressive ? 0 : videoSizeDefaults[2].value.int32);
    *height1 = videoSizeDefaults[3].value.int32;
    /* set F2 height to 0 if progressive, func returns -1 */
    *height2 = (progressive ? 0 : videoSizeDefaults[4].value.int32);
    *width = videoSizeDefaults[5].value.int32;

switch (timing) {
    case ML_TIMING_525:
        switch (rasterSize) {
            case NTSC_486: //
                *starty1 = 21;

```

```

        *starty2 = 283;
        *height1 = 243;
        *height2 = 243;
        break;
    }
    break;
}

```

Following are the ML control settings:

```

ML_VIDEO_TIMING_INT32 = ML_TIMING_525
ML_VIDEO_COLORSPACE_INT32 = ML_COLORSPACE_CbYCr_601_HEAD
ML_VIDEO_PRECISION_INT32 = 8
ML_VIDEO_START_Y_F1_INT32 = 21
ML_VIDEO_START_Y_F2_INT32 = 283
ML_VIDEO_HEIGHT_F1_INT32 = 243
ML_VIDEO_HEIGHT_F2_INT32 = 243
ML_IMAGE_TEMPORAL_SAMPLING_INT32 = ML_TEMPORAL_SAMPLING_FIELD_BASED
ML_VIDEO_SAMPLING_INT32 = ML_SAMPLING_422
ML_VIDEO_WIDTH_INT32 = 720
ML_IMAGE_WIDTH_INT32 = 720
ML_IMAGE_HEIGHT_1_INT32 = 486
ML_IMAGE_HEIGHT_2_INT32 = 0
ML_IMAGE_SAMPLING_INT32 = ML_SAMPLING_444
ML_IMAGE_COLORSPACE_INT32 = ML_COLORSPACE_RGB_601_FULL
ML_IMAGE_PACKING_INT32 = ML_PACKING_8
ML_IMAGE_INTERLEAVE_MODE_INT32 = ML_INTERLEAVE_MODE_INTERLEAVED
ML_IMAGE_DOMINANCE_INT32 = ML_DOMINANCE_F1
ML_IMAGE_ORIENTATION_INT32 = ML_ORIENTATION_TOP_TO_BOTTOM
XTDIGVID_LOOPBACK_INT32 = XTDIGVID_LOOPBACK_DISABLE
ML_IMAGE_COMPRESSION_INT32 = ML_COMPRESSION_UNCOMPRESSED
ML_IMAGE_ROW_BYTES_INT32 = 0
ML_IMAGE_SKIP_PIXELS_INT32 = 0
ML_IMAGE_SKIP_ROWS_INT32 = 0
ML_VIDEO_START_X_INT32 = 1

```

Programmable Lookup Tables (LUTs)

This device-specific example shows you how to use the LUTs to invert video. You can perform this example with 8-bit packings only (load with an inverse ramp). Following are the DMediaPro control settings:

```
for (i=1; i<=NUM_DEFINED_LUT_ENTRIES;i++)
lutentries[NUM_DEFINED_LUT_ENTRIES-i] = i;

pv->param = XTDIGVID_LUT_YG_INT32_ARRAY;
pv->value.pInt32 = lutentries;
pv->length=NUM_DEFINED_LUT_ENTRIES;
pv->maxLength=sizeof(lutentries)/sizeof(DMint32);
pv++;

pv->param = XTDIGVID_LUT_UB_INT32_ARRAY;
pv->value.pInt32 = lutentries;
pv->length=NUM_DEFINED_LUT_ENTRIES;
pv->maxLength=sizeof(lutentries)/sizeof(DMint32);
pv++;

pv->param = XTDIGVID_LUT_VR_INT32_ARRAY;
pv->value.pInt32 = lutentries;
pv->length=NUM_DEFINED_LUT_ENTRIES;
pv->maxLength=sizeof(lutentries)/sizeof(DMint32);
pv++;
```

FF Mode

For output transfers, you can use Field/Frame mode (FF mode) (XTDIGVID_FF_MODE_INT32) to assist an application in performing 3/2 pulldown. You can only use this mode when there are 1080p 23.97 frames in memory and you want to output 1080i 59.94 fields. By default FF mode is disabled. To enable FF mode, follow these steps:

1. Set XTDIGVID_FF_MODE_INT32 to the value XTDIGVID_FF_MODE_ENABLE.
2. Set the ML_IMAGE_INTERLEAVE_MODE_INT32 to ML_INTERLEAVE_MODE_INTERLEAVED.

In this special Field/Frame mode, you can send the DMediaPro Board an entire frame, but the board only extracts a single field. For example, if the 1080p frames in memory are labelled A,B,C..., and FF mode is enabled, you can send the board AAABBCCDD, and it will output field 1 from A, field 2 from A, field 1 from A, field 2 from B, and field 1 from B. Each buffer you send is treated as an interleaved frame, but only a single field is extracted from it. As a result, your application does not have to manually extract fields from the frames in memory.

UST (Unadjusted System Time) and MSC (Media Stream Count) function exactly as they do in the one-field-per buffer case; MSC increases by one for each buffer. To specify whether the first field is an F1 or an F2, use the ML_IMAGE_DOMINANCE_INT32 control.

The following device-specific example shows you how to allocate buffers for a fixed set of images and how to place the images in the buffer to achieve the desired results.

```
// buffer allocation
if (ffmode)
    bufferCount = imageCount*5/2;
else
    bufferCount = (imageCount > 1 ? imageCount : maxBuffers);

bufArray = (void *) malloc(bufferCount * sizeof(void *));
if (bufArray == NULL) {
    fprintf(stderr, "Cannot allocate buffer array\n");
    exit(-1);
}
else
    bzero(bufArray, (bufferCount * sizeof(void *)));
```

```
// filling the buffers in ffmode
if (ffmode) {
    /*
```

In field/frame mode, you must send each frame 2.5 times (on average), so you must duplicate entries in the buffer array. Begin with buffer array entries as follows:

ABCD.....

And finish with:

AAABBCCDD

```
*/
```

```
for(fnum = bufferCount-1; fnum>0; fnum--)
    bufArray[fnum] = bufArray[(int)(fnum*2/5)];
```

Setting Controls on a Jack

This section provides example code for setting up a jack control. The following example uses a jack control to enable a loopback on the HD input jack:

```
// enable loopback on HD input jack

#include <stdio.h>
#include <ML/ml.h>
#include <ML/mlu.h>
#include <ML/ml_xtdigvid.h>

int main( int argc, char **argv )
{
    DMstatus status;
    DMopenid jack;

    // open the HD input jack on the xt-digvid device
    {
        DMint64 sysId = ML_SYSTEM_LOCALHOST;
        DMint64 devId;
        DMint64 jackId;
```

```
char *jackName = "HDSerialDigitalInputJack";

if( status = dmufindDeviceByName( sysId, "xt-digvid", &devId )) {
fprintf( stderr, "xt-digvid: %s\n", dmStatusName( status ));
return( 1 );
}

if( status = dmufindJackByName( devId, jackName, &jackId )) {
fprintf( stderr, "%s: %s\n", jackName, dmStatusName( status ));
return( 1 );
}

if( status = dmOpen( jackId, NULL, &jack ) ) {
fprintf( stderr, "open %s: %s\n", jackName, dmStatusName( status
));
return( 1 );
}
}

// set the loopback control
{
DMpv ctrls[] = {
XTDIGVID_LOOPBACK_INT32, 0, 0, 0,
ML_END, 0, 0, 0
};

ctrls[ 0 ].value.int32 = XTDIGVID_LOOPBACK_ENABLE;

if( status = dmSetControls( jack, ctrls )) {
fprintf( stderr, "dmSetControls: %s\n", dmStatusName(status));
return( 1 );
}
}

dmClose( jack );
return 0;
}
```

Synchronizing Data Streams and Signals

You can use UST (Unadjusted System Time) and MSC (Media Stream Count) signals to synchronize data streams. These are special signals that are recognized or generated by the DMediaPro Board. For more information, see the *ML Programmer's Guide*.

Restrictions and Important Notes

1. You can only open one input path and one output path at the same time.
2. Before you configure a path with SetControls, your image controls and your video controls must be compatible. Because the DMedia Pro Board validates the path configuration at SetControl time, set all video controls and image controls at the same time. If this is inconvenient, start from a valid configuration and change "blocks" of controls. This alternative method also results in a valid path configuration.
3. The image width and height must correspond to the video width and height as follows:

- Progressive formats

`ML_IMAGE_WIDTH = ML_VIDEO_WIDTH`

`ML_IMAGE_HEIGHT_1 = ML_VIDEO_HEIGHT_F1`

`ML_IMAGE_HEIGHT_2 = 0`

- Interlaced formats with `ML_INTERLEAVE_MODE_INT32` set to `ML_INTERLEAVE_MODE_INTERLEAVED`

`ML_IMAGE_WIDTH = ML_VIDEO_WIDTH`

`ML_IMAGE_HEIGHT_1 = ML_VIDEO_HEIGHT_F1 +`

`ML_VIDEO_HEIGHT_F2`

`ML_IMAGE_HEIGHT_2 = 0`

- Interlaced formats with ML_INTERLEAVE_MODE_INT32 set to ML_INTERLEAVE_MODE_SINGLE_FIELD
ML_IMAGE_WIDTH = ML_VIDEO_WIDTH
ML_IMAGE_HEIGHT_1 = ML_VIDEO_HEIGHT_F1
ML_IMAGE_HEIGHT_2 = ML_VIDEO_HEIGHT_F2
4. The VBOB does not distinguish between 25PsF and 50i timings. There are three possible results:
- If the input timing is 25PsF, the detected input signal is 50i.
 - If the output timing is 25PsF and the genlock source is 25PsF, the detected genlock signal is 50i.
 - If the output timing is 50i and the genlock source is 25PsF, the detected genlock signal is 50i.

Index

Numbers

- 10-bit formats, 4
- 3/2 pulldown, 61
- 8-bit formats, 4

A

- ADAT In
 - device controls, 37
 - disabling AES, 38
- ADAT Out
 - device controls, 37
 - disabling AES, 38
- Advanced Television Standards Committee, 3
- AES 1/2 output
 - Octane2, 33, 34
 - Onyx 3000, 35
 - Origin 3000, 35
- AES 3/4 output
 - Octane2, 34
 - Onyx 3000, 35
 - Origin 3000, 35
- AES device controls
 - displaying, 37
- AES In
 - device controls, 37
 - disabling ADAT, 38
 - setting default, 37
 - signal path, 38
- AES Out
 - device controls, 37
 - disabling ADAT, 38
 - setting default, 37
 - signal path, 38
- airflow
 - hardware cooling, 32
- alpha channel, 5, 75
- analog sync source
 - genlocking, 31
- applications
 - developing, 12, 45
- ATSC
 - video formats, 3
- audio panel
 - default menu, 37
 - input source, 38
 - output destination, 38
 - set up, 37-43
- audio synchronization
 - on Octane2, 33-34, 40
 - on Onyx 3000, 35-36, 41-43
 - on Onyx2, 35
 - on Origin 2000, 35
 - on Origin 3000, 35-36, 41-43
 - optional configurations, 44
- auto detect
 - Genlock, 72
 - input, 69
 - SYNC_LOST, 69

B

- backward compatibility, 86
- blank panel
 - removing, 20-21
- blanking
 - output, 76
- breakout cable, 34
- buffers
 - address, 53
 - bytes, 55
 - input image memory, 50-52
 - output image memory, 50-52
 - pixels, 55
 - repeating, 61
 - rows, 55
 - size, 54
- bytes
 - image memory buffer, 55

C

- cables
 - breakout, 34
 - input/output, 31-32
 - LVDS, 2, 30
 - monitor, 14
 - routing, 32
 - XIO Tri-Module, 14
- capturing 487 line 525, 84
- capturing graphics to video
 - described, 80
- CCIR formats, 3, 75
- CD
 - programming examples, 46
 - shipment components, 10
 - software installation, 12
- coaxial digital input, 33

- color model
 - listed, 74-75
- color space
 - color model, 74-75
 - conversion, 75
 - defined, 57
 - described, 55, 74
 - LUTs, 76
 - video data, 57
- components, 10
- compression
 - images, 54
- compression connector
 - identifying, 16
- compression connector caps
 - placing, 16, 19
 - removing, 23, 24
- connectors
 - compression, 16
 - displayed, 2
 - Genlock, 31
 - LVDS, 30
 - VBOB, 3
- control of blanking, 76
- controls
 - jack, 48-49
 - path, 47

D

- default input
 - setting, 37
- default output
 - setting, 37
- device controls
 - displaying, 37
- Digital Audio Board. See PCI Digital Audio Board DM2/DM3 Boards. See DMediaPro Board

- DMediaPro Board
 - attaching to Tri-Module, 22-23
 - connecting to VBOB, 29-32
 - connectors, 2
 - described, xiii, 2, 6-7
 - features, 5
 - Genlock auto detect, 72
 - input timing auto detect, 69
 - installing in Octane2, 9, 13
 - operating system, 12
 - SetControls, 92
 - shipment components, 10
 - software installation, 12
 - theory of operation, 6-7
 - DMediaPro Board Controls
 - HD default input path, 65
 - HD default output path, 66
 - input/output image memory buffer, 50-52
 - input/output video paths, 50-52
 - jack, 48-49
 - path, 47
 - SD default input path, 65
 - SD default output path, 67
 - DMediaPro Board Diagram, 7
 - DMediaPro Board LEDs, 2
 - DMediaPro Board Panel, 2
 - DMediaPro CD
 - programming examples, 46
 - software installation, 12
 - DMediaPro Events
 - defined, 81
 - DMediaPro software
 - installing, 12
 - Downloadable Lookup Tables
 - discussed, 7
- E**
- EE mode
 - changing, 48
 - described, 79
 - jack controls, 48
 - transfers, 48
 - electrical signal paths, 38
 - events
 - defined, 58, 81
 - examples
 - capturing 487 line 525, 84
 - color space conversion, 77
 - FF mode, 89
 - LUTs, 88
 - playback from memory to video, 85
 - programming, 46, 84
 - re-sizing field height, 86
 - setting jack controls, 90
- F**
- FF mode
 - 3/2 pulldown, 61
 - fiber channel board
 - requirements, 9, 33
 - field dominance
 - described, 78-79
 - field height
 - re-sizing, 86
 - field size
 - programmable, 5
 - formats
 - described, 4
 - frame rate
 - video timings, 4

G

- gamma correction
 - LUTs, 76
 - support, 5
- Genlock
 - connecting cables, 31
 - described, 69
 - EE mode, 79
 - loop-throughs, 31
 - set up, 69
 - VBOB, 3
- Genlock auto detect
 - described, 72
- Genlock input signal
 - identifying, 72
- Genlock input timings
 - listed, 70-71
- Genlock jack
 - timing ID, 83
- Genlock signal type
 - described, 59
- Genlock source timing
 - described, 60
 - locking, 72
- Genlock sync lock, 81
- Genlock sync source
 - setting, 59
- getControls
 - Genlock state, 63
 - Genlock timing, 62
- graphics board
 - requirements, 9
 - V10/V12, 11, 13
 - verifying installation, 11
- graphics input
 - XTDIGVID_LOOPBACK, 52
- graphics to video
 - capturing, 80

H

- hardware inventory list
 - checking graphics board, 11
 - verifying installation, 27
- HD
 - default input path controls, 65
 - default output path controls, 66
 - formats, 3
 - input/output paths, 50
 - output and Genlock, 69
 - output and Genlock input timings, 70
- HD EE mode, 48
- HD Genlock In
 - analog sync source, 31
- HD GVO Board
 - capturing graphics to video, 80
- HD input jack
 - enabling loopback, 90
- HD serial digital input
 - jack controls, 48
 - path controls, 47
- HD serial digital output
 - jack controls, 48
 - path controls, 47
- HD video jack
 - path controls, 47
- headroom range, 75
- heat sinks, 14
- high definition. See HD
- horizontal phase adjustment, 5
- house sync generator
 - Octane2, 33
 - Onyx 3000, 35
 - Origin 3000, 35
 - PCI Digital Audio Board, 44

I

- I-Brick
 - PCI Digital Audio Board, 35
- image height, 53
- image memory buffer
 - bytes, 55
 - pixels, 55
 - rows, 55
 - size, 56
- image parameters. See ML_IMAGE_parameters
- images
 - height, 92
 - interleaved, 53
 - ML, 12
 - order, 55
 - width, 53, 92
 - XTDIGVID, 12
- input
 - colorspace, 57
 - connectors, 3
 - default, 37
 - VBOB, 3
- input device
 - menu, 38
 - setting default, 37
- input image memory buffer
 - DMediaPro Board Controls, 50-52
- input path
 - opening, 92
- input signal path
 - setting, 38
- input timing auto detect
 - described, 69
 - SYNC_LOST, 69
- input video paths
 - colorspace, 57
 - DMediaPro Board Controls, 50-52

- installation
 - in Octane2, 13
 - PCI Digital Audio Board, 33-34
 - requirements, xiii, 9
 - software, 12
 - verifying, 12, 27
- interlaced formats, 4
 - described, 4
 - frame boundaries, 56
 - height, 92
 - interleave mode, 93
 - output underflow, 80
 - video height, 58
 - width, 92
- interlaced images
 - interleave mode, 56
- interleaved images
 - image height, 53
- internal audio
 - default devices, 37
 - on Octane2, 33, 40
- I/O. See input/output
- IRIX 6.5.11
 - installation, 12
- ITU-R BT.601-5
 - color model support, 74
- ITU-R BT.709-2
 - color model support, 74
- ITU-R formats, 3

J

- jack controls
 - EE mode, 48-49
 - setting up, 90
 - transfer, 48

K

key scaling, 5

L

LEDs

displayed, 2

Lookup Tables. See LUTs

LUTS

inverting video, 88

LUTs

color space, 76

discussed, 7

example, 88

gamma correction, 76

values, 58

LVDS

EE mode, 79

XTDIGVID_LOOPBACK, 62

LVDS cables

connecting, 30

displayed, 2

M

maximum value, 74

media stream count

defined, 56

FF mode, 89

synchronizing data streams, 92

memory

data transfer, 47, 48

path set up, 47

queue, 64

requirements, 9

RGB, 5

memory to video

jack controls, 48

path, 47

transfer example, 85

minimum value, 74

ML, 59

installing images, 12

library., 45

programming examples, 46

ML_COLORSPACE

color conversion values, 76

described, 55, 74

example, 77

LUTs, 76

video data, 57

ML_COMPRESSION_UNCOMPRESSED

image compression, 54

ML_DEVICE_EVENTS

input/output path, 51

use, 58

values, 58

ML_DEVICE_STATE

input/output path, 51

use, 58

value, 58

ML_DOMINANCE

frame boundaries, 56

ML_DOMINANCE_F2, 56

ML_EVENT_VIDEO_SEQUENCE_LOST

described, 81

ML controls, 82

ML_DEVICE_EVENTS values, 58

ML_EVENT_VIDEO_SYNC_GAINED

described, 81

input path, 82

ML_DEVICE_EVENTS values, 58

output path, 82

- ML_EVENT_VIDEO_SYNC_LOST
 - described, 81
 - error status values, 83
 - input path, 82
 - input timing auto detect, 69
 - ML_DEVICE_EVENTS values, 58
 - output path, 82, 83
 - XTDIGVID_GENLOCK_ERROR_STATUS, 63
- ML_IMAGE_BUFFER_POINTER
 - input/output path, 50
 - use, 53
- ML_IMAGE_BUFFER_SIZE
 - input/output path, 50
 - use, 56
 - value, 56
- ML_IMAGE_COLORSPACE
 - input/output path, 50
 - use, 55
 - values, 55
- ML_IMAGE_COMPRESSION
 - input/output path, 50
 - use, 54
 - value, 54
- ML_IMAGE_DOMINANCE
 - input/output path, 50
 - use, 56
 - values, 56
- ML_IMAGE_HEIGHT_1
 - input/output path, 50
 - use, 53
 - value, 53
- ML_IMAGE_HEIGHT_2
 - input/output path, 50
 - use, 53
 - value, 53
- ML_IMAGE_INTERLEAVE_MODE
 - input/output path, 50
 - interlaced images, 56
 - use, 56
- ML_IMAGE_ORIENTATION
 - capturing graphics to video, 80
 - input/output path, 50
 - use, 55
 - values, 55
- ML_IMAGE_PACKING, ??-5
 - format, 54
 - input/output path, 50
 - supported modes, 5-??
 - values, 54
 - VL conversions, 72
- ML_IMAGE_ROW_BYTES
 - input/output path, 50
 - range, 55
 - use, 55
- ML_IMAGE_SAMPLING
 - input/output path, 50
 - packing modes, 5-??
 - use, 54
 - values, 54
 - VL conversions, 72
- ML_IMAGE_SKIP_PIXELS
 - input/output path, 50
 - range, 55
 - use, 55
- ML_IMAGE_SKIP_ROWS
 - input/output path, 50
 - range, 55
 - use, 55
- ML_IMAGE_TEMPORAL_SAMPLING
 - input/output path, 50
 - use, 56
 - values, 56
- ML_IMAGE_WIDTH
 - input/output path, 50
 - ML_VIDEO_WIDTH, 58
 - value, 53
- ML_INTERLEAVE_MODE
 - image height, 53
 - values, 56

- ML_INTERLEAVE_MODE_SINGLE_FIELD, 56
- ML_MODE_RWE
 - open mode, 63
- ML_OPEN_MESSAGE_PAYLOAD_SIZE
 - input/output path, 52
 - range, 64
 - use, 64
- ML_OPEN_MODE
 - input/output path, 52
 - use, 63
 - value, 63
- ML_OPEN_RECEIVE_QUEUE_COUNT
 - input/output path, 52
 - range, 64
 - use, 64
- ML_OPEN_SEND_QUEUE_COUNT
 - input/output path, 52
 - range, 64
 - use, 64
- ML_OPEN_SEND_SIGNAL_COUNT
 - input/output path, 52
 - range, 64
 - use, 64
- ML_ORIENTATION
 - image order, 55
- ML_ORIENTATION_BOTTOM_TO_TOP, 55
- ML_PACKING
 - supported modes, 5-??
- ML_QUEUE_RECEIVE_COUNT
 - input/output path, 51
 - use, 59
 - value, 59
- ML_QUEUE_RECEIVE_WAITABLE
 - input/output path, 51
 - use, 59
 - value, 59
- ML_QUEUE_SEND_COUNT
 - input/output path, 51
 - use, 59
 - value, 59
- ML_QUEUE_SEND_WAITABLE
 - input/output path, 51
 - use, 59
 - value, 59
- ML_RANGE_FULL
 - defined, 55
- ML_RANGE_HEAD
 - defined, 55
- ML_SAMPLING
 - image sampling values, 54
 - packing modes, 5-??
 - video data, 57
- ML_TIMING
 - changing from SD to HD, 68
 - defined, 57
 - described, 68
 - field descriptions, 68
 - Genlock jack, 62
 - Genlock source, 60
 - input jack, 63
 - ML_VIDEO_SIGNAL_PRESENT, 63
- ML_TIMING_525
 - HD Genlock input, 69
 - SD Genlock input, 69
- ML_TIMING_625
 - HD Genlock input, 69
 - SD Genlock input, 69
- ML_VIDEO_COLORSPACE
 - input/output path, 50
 - use, 57
 - values, 57
- ML_VIDEO_GENLOCK_SIGNAL_PRESENT
 - output path, 52
 - use, 62
 - values, 62, 83
- ML_VIDEO_GENLOCK_SOURCE_TIMING
 - enabling auto detect, 72
 - output path, 51
 - use, 60
 - values, 60

- ML_VIDEO_GENLOCK_TYPE
 - output path, 51
 - use, 59
 - values, 59
- ML_VIDEO_H_PHASE
 - output path, 51
 - use, 60
 - value, 60
- ML_VIDEO_HEIGHT_F1
 - input/output path, 51
 - use, 58
 - values, 58
- ML_VIDEO_HEIGHT_F2
 - input/output path, 51
 - use, 58
 - value, 58
- ML_VIDEO_MSC
 - input/output path, 50
 - use, 56
 - value, 56
- ML_VIDEO_OUTPUT_REPEAT
 - described, 80
 - output path, 51
 - use, 61
 - values, 61, 80
- ML_VIDEO_PRECISION
 - input/output path, 50
 - range, 57
 - use, 57
- ML_VIDEO_REPEAT
 - DMLbuffers, 61
- ML_VIDEO_SAMPLING
 - input/output path, 51
 - use, 57
 - values, 57
- ML_VIDEO_SIGNAL_PRESENT
 - input path, 52
 - use, 63
 - values, 63
- ML_VIDEO_START_X
 - input/output path, 51
 - range, 57
 - use, 57
- ML_VIDEO_START_Y_F1
 - input/output path, 51
 - use, 58
 - value, 58
- ML_VIDEO_START_Y_F2
 - input/output path, 51
 - use, 58
 - value, 58
- ML_VIDEO_TIMING
 - Genlock source, 60
 - input/output path, 50
 - use, 57
 - values, 57
- ML_VIDEO_UST
 - input/output path, 50
 - use, 56
 - value, 56
- ML_VIDEO_V_PHASE
 - output path, 51
 - use, 60
 - value, 60
- ML_VIDEO_WIDTH
 - input/output path, 51
 - use, 58
 - value, 58
- MLbuffers
 - output underflow, 61
- monitor cable
 - reconnecting, 26
 - removing, 14
- MSC
 - defined, 56
 - FF mode, 89
 - synchronizing data streams, 92

N

natural graphics order, 55

natural video order, 55

NTSC

field height, 86

video timings, 4

O**Octane2**

and DMediaPro, xiii

DMediaPro Board installation, 9, 13

powering off, 13

powering on, 26

removing monitor cable, 14

synchronizing audio, 33-34, 40

Onyx 3000

and field installation, xiii

field installation, 9

synchronizing audio, 35-36, 41-43

VBOB, 32

Onyx2

PCI Digital Audio board, 35

open mode, 63

OpenGL

capturing graphics to video, 80

operating system

requirements, xiii

upgrading, 12

verifying installation, 12

optical signal paths, 38

option board

removing, 20-21

order

image packing, 54

Origin 2000

PCI Digital Audio Board, 35

Origin 3000

field installation, 9

synchronizing audio, 35-36, 41-43

VBOB, 32

output

3/2 pulldown mode, 5

connectors, 3

default, 37

horizontal phase adjustment, 5

VBOB, 3

vertical phase adjustment, 5

output device

preferences, 39

selecting default, 37

sync source, 40

output device menu, 38

output image memory buffer

DMediaPro Board Controls, 50-52

output path

colorspace, 57

Genlock source timing, 60

opening, 92

output signal path

setting, 38

output sync source

setting, 39

P

packing format

described, 54

packing modes

supported, 5-??

PAL

video timings, 4

- path
 - configuring, 92
 - HD input/output, 50-52
 - memtovid, 47
 - opening, 92
 - SD input/output, 50-52
 - setting up, 47
 - vidtomem, 47
 - path controls
 - described, 47
 - HD default input, 65
 - HD default output, 66, 67
 - SD default input, 65
 - SD default output, 67
 - payload area, 64
 - P-Brick
 - PCI Digital Audio Board, 35
 - PCI Digital Audio Board
 - breakout cable, 34
 - house sync generator, 44
 - installing, 33-34
 - single board
 - synchronizing on Onyx 3000, 35, 41
 - synchronizing on Origin 3000, 35, 41
 - two boards
 - synchronizing on Onyx 3000, 35, 42
 - synchronizing on Origin 3000, 35, 42
 - PCI module
 - requirements, 9
 - phase adjustment, 5
 - pixel clocks
 - video formats, 3
 - pixels
 - image memory buffer, 55
 - image sampling, 54
 - powering off, 13
 - powering on, 26
 - precision, 57
 - processor
 - requirements, 9
 - product support, xv
 - programmable field size, 5
 - programmable lookup table. See LUTs
 - programming
 - basics, 46
 - examples, 46, 84
 - progressive formats
 - height, 92
 - interleave mode, 53
 - output underflow, 80
 - video height, 58
 - width, 92
 - progressive frame formats
 - described, 4
 - progressive segmented frame formats
 - described, 4
 - video height, 58
 - progressive signals
 - frame start, 58
 - progressive timings, 78
 - PsF formats
 - described, 4
 - video height, 58
 - publications
 - and shipment, xiv
 - pulldown mode, 5
- Q**
- queue
 - described, 59
 - memory, 64
- R**
- read only
 - input/output path, 50, 52

Rec. 601
color model support, 74
color space conversion, 5
formats, 3

Rec. 709
color model support, 74

reclocking, 79

RGB
color space, 75
LUTs, 76
memory, 5
video interace, 5

rounding, 76

rows
image memory buffers, 55

RWE mode, 63

S

sampling
packing modes, 5-??
video jack, 57

SD
default input path controls, 65
default output path controls, 67
formats, 3
input/output paths, 50
output and Genlock, 69
re-sizing field height, 86

SD EE mode, 48

SD Genlock In
analog sync source, 31

SD serial digital input
jack controls, 48
path controls, 47

SD serial digital output
jack controls, 48
path controls, 47

SD video jack
path controls, 47

SDI, 3

serial digital interface, 3

serial input
XTDIGVID_LOOPBACK, 52

SetControls
path configuration, 92

shipment
and publications, xiv
cables, 2
components, 10

signal path
setting, 38

size
image packing, 54

SMPTE 240M
color model support, 74

SMPTE 274M
fields and frames, 78

SMPTE formats, 3

software
installing, 12

standard definition. See SD

static electricity, 15

support, xv

sync source
setting, 39
video, 44

SYNC_LOST
described, 81
input timing auto detect, 69
ML_DEVICE_EVENTS, 58
XTDIGVID_GENLOCK_ERROR_STATUS, 63

synchronization
 data streams, 92
 on Octane2, 33-34, 40
 on Onyx 3000, 35-36, 41-43
 on Onyx2, 35
 on Origin 2000, 35
 on Origin 3000, 35-36, 41-43
 optional configurations, 44
 system
 upgrading, 12
 verifying installation, 12

T

technical support, xv
 temporal sampling, 56
 timestamp, 56
 timing
 defined, 57
 genlock input, 70-71
 Genlock jack, 62
 restrictions, 93
 video output, 70-71
 transfer
 jack controls, 48
 type
 image packing, 54

U

unadjusted system time. See UST
 UST, 5
 defined, 56
 FF mode, 89
 synchronizing data streams, 92

V

VBOB
 connecting, 29-32
 Genlock, 3
 input, 3
 LVDS cables, 2
 output, 3
 timing restrictions, 93
 vertical phase adjustment, 5
 video
 height, 92
 inverting, 88
 supported formats, 3
 width, 58, 92
 video formats, 3
 video output timing
 listed, 70-71
 video parameters. See ML_VIDEO_parameters
 video signal
 horizontal phase, 60
 vertical phase, 60
 video timings
 frame rate, 4
 video to memory
 path, 47
 VPro Graphics Board
 installation requirements, 9
 V10/V12, 11, 13
 verifying installation, 11

W

width
 video, 58
 workstation. See Octane2
 wrist strap
 attaching, 15
 shipment components, 10

X

- XIO option board
 - removing, 20-21
- XIO Tri-Module
 - aligning, 24, 25
 - displayed, 19
 - heat sinks, 14
 - re-installing, 24-26
 - releasing, 18
 - removing, 16, 17-19
 - removing cables, 14
- XIO Tri-Module cables, 14
- XIO Tri-Module handles, 18
- XIO Tri-Module screws
 - removing, 17
- XTDIGVID
 - installing images, 12
- XTDIGVID_EE_MODE
 - changing during transfer, 48
 - described, 79
 - output path, 51
 - use, 61
 - values, 61
- XTDIGVID_FF_MODE
 - described, 89
 - example, 89
 - output path, 51
 - use, 61
 - values, 61
- XTDIGVID_GENLOCK_ERROR_STATUS
 - output path, 52
 - use, 63
 - values, 63, 83
- XTDIGVID_GENLOCK_STATE
 - output path, 52
 - use, 63
 - value, 63

- XTDIGVID_LOOPBACK
 - input path, 52
 - use, 62
- XTDIGVID_LUT_UB
 - input/output path, 51
 - inverting video, 88
 - use, 58
 - value, 58
- XTDIGVID_LUT_VR
 - input/output path, 51
 - inverting video, 88
 - use, 58
 - value, 58
- XTDIGVID_LUT_YG
 - input/output path, 51
 - inverting video, 88
 - use, 58
 - value, 58

Y

- YCrCb
 - headroom range, 75
- YUV
 - full range, 75